

# Compal Confidential

*Lotus AMD M/B LA8731P Schematics Document*

*AMD Trinity APU / Hudson FCH M3*

[www.aitech1.ru](http://www.aitech1.ru)

*Date : 2011-12-27*

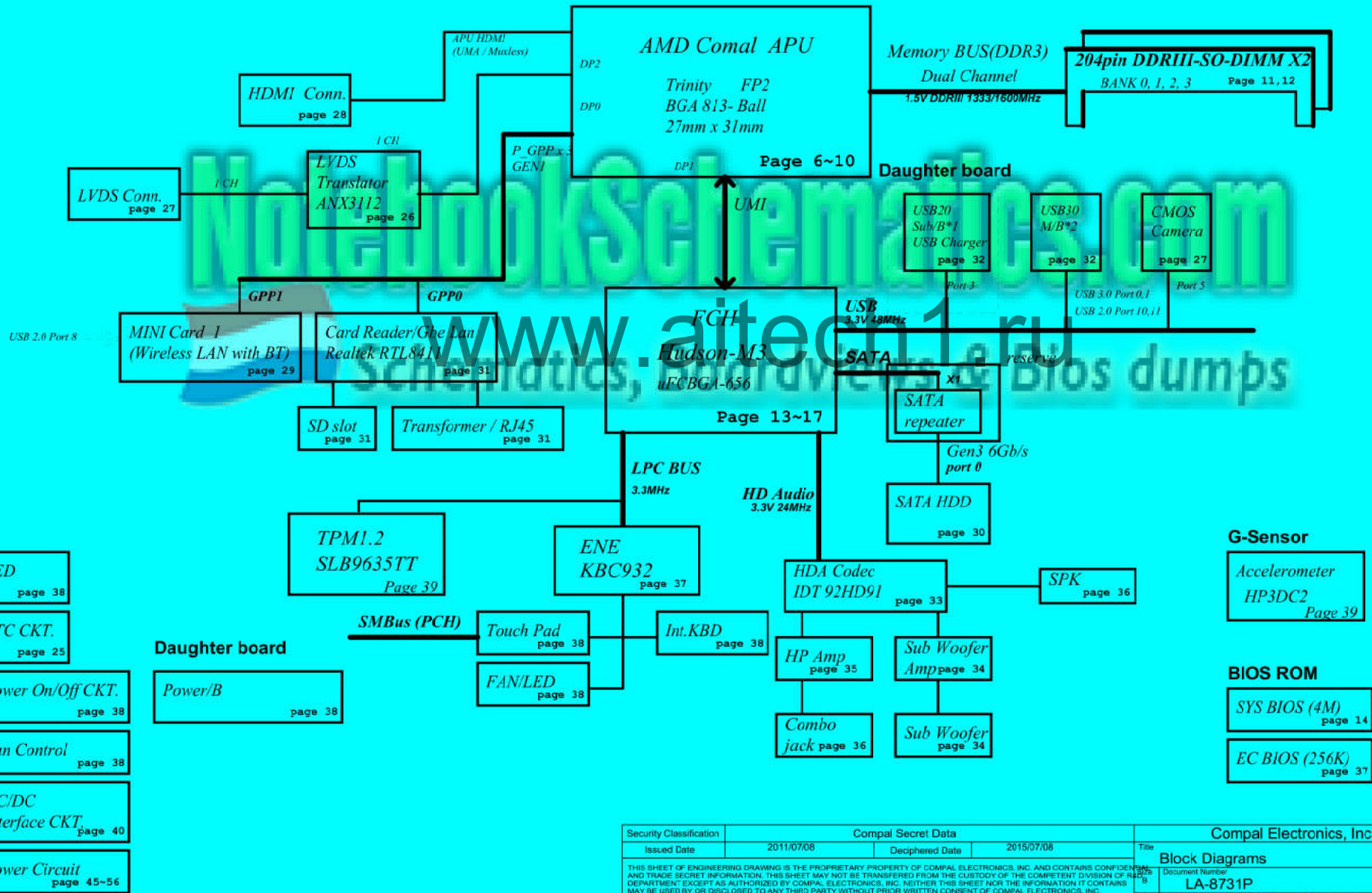
*Version 0.1*

|   |                    |                 |            |                          |                            |
|---|--------------------|-----------------|------------|--------------------------|----------------------------|
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|   |                    |                 |            | LA-8731P                 |                            |
|   |                    |                 |            | Date:                    | Tuesday, December 27, 2011 |
|   |                    |                 |            | Sheet                    | 1 of 47                    |
|   |                    |                 |            | Rev                      | 0.1                        |

# Compal Confidential

Model Name : QAU51 AMD

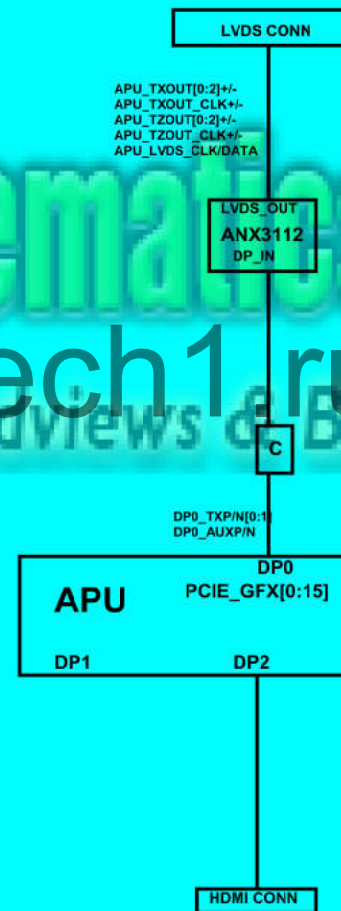
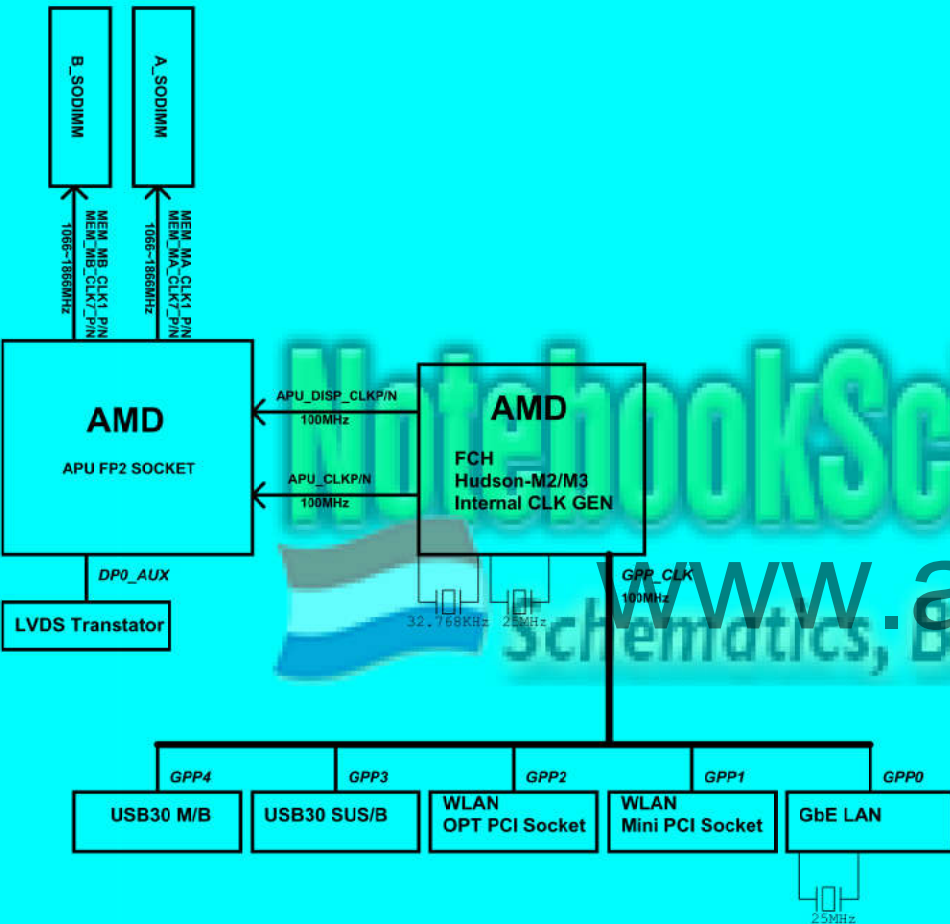
## AMD Comal



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|   |            |                    |            | Rev                      | 0.1                        |

## CLOCK DISTRIBUTION

## DISPLAY OUTPUT



|   |                            |                 |                          |                              |
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| Size  | Juston                     | Document Number | LA-8731P                 | Rev                          |
| Date  | Tuesday, December 27, 2011 | Sheet           | 3                        | of 47                        |



## Voltage Rails

| Power Plane  | Description                                  | S1  | S3  | S5  |
|--------------|--|-----|-----|-----|
| VIN          | Adapter power supply (19V)                   | N/A | N/A | N/A |
| B+           | AC or battery power rail for power circuit.  | N/A | N/A | N/A |
| +CPU_CORE    | Core voltage for CPU                         | ON  | OFF | OFF |
| +CPU_CORE_NB | Voltage for On-die VGA of APU                | ON  | OFF | OFF |
| +VGA_CORE    | 0.95-1.2V switched power rail                | ON  | OFF | OFF |
| +VDDCI       | 0.95-1.2V switched power rail                | ON  | OFF | OFF |
| +0.75VS      | 0.75V switched power rail for DDR terminator | ON  | ON  | OFF |
| +1.0VSG      | 1.0V switched power rail for VGA             | ON  | OFF | OFF |
| +1.1ALW      | 1.1V switched power rail for FCH             | ON  | ON  | ON* |
| +1.1VS       | 1.1V switched power rail for FCH             | ON  | OFF | OFF |
| +1.2VS       | 1.2V switched power rail for APU             | ON  | OFF | OFF |
| +1.5V        | 1.5V power rail for CPU VDDIO and DDR        | ON  | ON  | OFF |
| +1.5VS       | 1.5V switched power rail                     | ON  | OFF | OFF |
| +1.8VSG      | 1.8V switched power rail                     | ON  | OFF | OFF |
| +2.5VS       | 2.5V for CPU_VDDA                            | ON  | OFF | OFF |
| +3VALW       | 3.3V always on power rail                    | ON  | ON  | ON* |
| +3V_LAN      | 3.3V power rail for LAN                      | ON  | ON  | ON  |
| +3VS         | 3.3V switched power rail                     | ON  | OFF | OFF |
| +5VALW       | 5V always on power rail                      | ON  | ON  | ON* |
| +5VS         | 5V switched power rail                       | ON  | OFF | OFF |
| +VSB         | VSB always on power rail                     | ON  | ON  | ON* |
| +RTCVCC      | RTC power                                    | ON  | ON  | ON  |

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## Audio Codec SSID

| Platform      | Platform ID |
|---------------|-------------|
| Evora 1.0 UMA | 0x18DE      |

x = 1 is read cmd, x = 0 is write cmd.

## External PCI Devices

| Device | IDSEL# | REQ#/GNT# | Interrupts |
|--------|--------|-----------|------------|
|        |        |           |            |
|        |        |           |            |
|        |        |           |            |
|        |        |           |            |
|        |        |           |            |

## EC SM Bus1 address

| Device        | Address     | HEX | Device               | Address     | HEX |
|---------------|-------------|-----|----------------------|-------------|-----|
| Smart Battery | 0001 011X b | 16H | ADI ADM1032 (GPU)    | 1001 101X b | 9AH |
|               |             |     | SB-TSI (APU)         | 1001 100X b | 98H |
|               |             |     | LVDS TR( RTD-2132S)  | 1010 100X b | A8H |
|               |             |     | VGA Internal Thermal | 1000 001X b | 82H |

## FCH SM Bus 0 address

| Device    | Address     | HEX | Device | Address | HEX |
|-----------|-------------|-----|--------|---------|-----|
| DDR DIMM1 | 1101 000X b | 90  |        |         |     |
| DDR DIMM2 | 1101 001X b | 94  |        |         |     |
|           |             |     |        |         |     |
|           |             |     |        |         |     |

## FCH SM Bus 1 address

| Device | Address | HEX | Device | Address | HEX |
|--------|---------|-----|--------|---------|-----|
|        |         |     |        |         |     |
|        |         |     |        |         |     |
|        |         |     |        |         |     |
|        |         |     |        |         |     |

| STATE                 | SIGNAL | SLP_S1# | SLP_S3# | SLP_S4# | SLP_S5# | +VALW | +V  | +VS | Clock |
|-----------------------|--------|---------|---------|---------|---------|-------|-----|-----|-------|
| Full ON               |        | HIGH    | HIGH    | HIGH    | HIGH    | ON    | ON  | ON  | ON    |
| S1 (Power On Suspend) |        | LOW     | HIGH    | HIGH    | HIGH    | ON    | ON  | ON  | LOW   |
| S3 (Suspend to RAM)   |        | LOW     | LOW     | HIGH    | HIGH    | ON    | ON  | OFF | OFF   |
| S4 (Suspend to Disk)  |        | LOW     | LOW     | LOW     | HIGH    | ON    | OFF | OFF | OFF   |
| S5 (Soft OFF)         |        | LOW     | LOW     | LOW     | LOW     | ON    | OFF | OFF | OFF   |

## Board ID / SKU ID Table for AD channel

|          |              |             |             |             |
|----------|--------------|-------------|-------------|-------------|
| Vcc      | 3.3V +/- 5%  |             |             |             |
| Ra/Rc/Re | 100K +/- 5%  |             |             |             |
| Board ID | Rb / Rd / Rf | VAD_BID min | VAD_BID typ | VAD_BID max |
| 0        | 0            | 0 V         | 0 V         | 0 V         |
| 1        | 8.2K +/- 5%  | 0.216 V     | 0.250 V     | 0.289 V     |
| 2        | 18K +/- 5%   | 0.436 V     | 0.503 V     | 0.538 V     |
| 3        | 33K +/- 5%   | 0.712 V     | 0.819 V     | 0.875 V     |
| 4        | 56K +/- 5%   | 1.036 V     | 1.185 V     | 1.264 V     |
| 5        | 100K +/- 5%  | 1.453 V     | 1.650 V     | 1.759 V     |
| 6        | 200K +/- 5%  | 1.935 V     | 2.200 V     | 2.341 V     |
| 7        | NC           | 2.500 V     | 3.300 V     | 3.300 V     |

## BOM Option Table

| BOM Structure | Description |
|---------------|-------------|
|---------------|-------------|

## BOM Config

| UMA |
|-----|
|-----|

## USB Port Table

| USB 2.0 | USB 1.1 | Port | 1 External USB Port |
|---------|---------|------|---------------------|
|         | UHCI0   | 0    | USB2.0 (left side)  |
|         |         | 1    |                     |
| EHCI1   | UHCI1   | 2    |                     |
|         |         | 3    |                     |
|         | UHCI2   | 4    |                     |
|         |         | 5    | Camera              |
|         |         | 6    |                     |
|         | UHCI3   | 7    |                     |
|         |         | 8    |                     |
|         | UHCI4   | 9    | BT                  |
| EHCI2   |         | 10   | USB2.0 (Right side) |
|         | UHCI5   | 11   | USB2.0 (Right side) |
|         |         | 12   |                     |
|         | UHCI6   | 13   |                     |

| USB 3.0 | Port | 1 External USB Port |
|---------|------|---------------------|
|         | 0    | USB3.0 (Right side) |
|         | 1    | USB3.0 (Right side) |
|         | 2    |                     |
|         | 3    |                     |

## SMBUS Control Table

|                          | SOURCE | BATT | Charger | HP Amp | MINI3 | SODIMM | EC_SMB_CK2<br>EC_SMB_DA2 | EC_SMB_CK1<br>EC_SMB_DA1 | G-Sensor | TP |
|--------------------------|--------|------|---------|--------|-------|--------|--------------------------|--------------------------|----------|----|
| EC_SMB_CK1<br>EC_SMB_DA1 | KB932  | V    | V       |        |       |        |                          |                          | V        |    |
| EC_SMB_CK2<br>EC_SMB_DA2 | KB932  |      |         | V      |       |        |                          |                          |          |    |
| FCH_SCLK0<br>FCH_SDATA0  | FCH    |      |         |        |       | V      |                          |                          |          |    |
| FCH_SCLK1<br>FCH_SDATA1  | FCH    |      |         |        |       |        |                          |                          |          | V  |

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| Notes List  |                    |                 |                            |
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## UCPU1A

GPU

Delete GPU  
1202 CalvinGLAN/Card reader  
WLAN

UMI

23 PCIE\_DTX\_C\_FRX\_P0  
23 PCIE\_DTX\_C\_FRX\_N0  
21 PCIE\_DTX\_C\_FRX\_P1  
21 PCIE\_DTX\_C\_FRX\_N1

13 UMI\_MTX\_C\_FRX\_P0  
13 UMI\_MTX\_C\_FRX\_N0  
13 UMI\_MTX\_C\_FRX\_P1  
13 UMI\_MTX\_C\_FRX\_N1  
13 UMI\_MTX\_C\_FRX\_P2  
13 UMI\_MTX\_C\_FRX\_N2  
13 UMI\_MTX\_C\_FRX\_P3  
13 UMI\_MTX\_C\_FRX\_N3

 P\_VDDP W/S=8/12 mil, <3000mil

|     |               |               |     |
|-----|---------------|---------------|-----|
| AP1 | P_GFX_RXP[0]  | P_GFX_TXP[0]  | AN1 |
| AP2 | P_GFX_RXN[0]  | P_GFX_TXN[0]  | AN2 |
| AM1 | P_GFX_RXP[1]  | P_GFX_TXP[1]  | AM4 |
| AM2 | P_GFX_RXN[1]  | P_GFX_TXN[1]  | AM3 |
| AK3 | P_GFX_RXP[2]  | P_GFX_TXP[2]  | AK2 |
| AK4 | P_GFX_RXN[2]  | P_GFX_TXN[2]  | AK1 |
| AI1 | P_GFX_RXP[3]  | P_GFX_TXP[3]  | AH1 |
| AJ2 | P_GFX_RXN[3]  | P_GFX_TXN[3]  | AH2 |
| AH4 | P_GFX_RXP[4]  | P_GFX_TXP[4]  | AE3 |
| AH3 | P_GFX_RXN[4]  | P_GFX_TXN[4]  | AE4 |
| AE2 | P_GFX_RXP[5]  | P_GFX_TXP[5]  | AE1 |
| AE1 | P_GFX_RXN[5]  | P_GFX_TXN[5]  | AE2 |
| AD1 | P_GFX_RXP[6]  | P_GFX_TXP[6]  | AD4 |
| AD2 | P_GFX_RXN[6]  | P_GFX_TXN[6]  | AD3 |
| AB3 | P_GFX_RXP[7]  | P_GFX_TXP[7]  | AB2 |
| AB4 | P_GFX_RXN[7]  | P_GFX_TXN[7]  | AB1 |
| AA1 | P_GFX_RXP[8]  | P_GFX_TXP[8]  | Y1  |
| AA2 | P_GFX_RXN[8]  | P_GFX_TXN[8]  | Y2  |
| V4  | P_GFX_RXP[9]  | P_GFX_TXP[9]  | V3  |
| V3  | P_GFX_RXN[9]  | P_GFX_TXN[9]  | V4  |
| V2  | P_GFX_RXP[10] | P_GFX_TXP[10] | U1  |
| V1  | P_GFX_RXN[10] | P_GFX_TXN[10] | U2  |
| T1  | P_GFX_RXP[11] | P_GFX_TXP[11] | T4  |
| T2  | P_GFX_RXN[11] | P_GFX_TXN[11] | T3  |
| P3  | P_GFX_RXP[12] | P_GFX_TXP[12] | P2  |
| P4  | P_GFX_RXN[12] | P_GFX_TXN[12] | P1  |
| N1  | P_GFX_RXP[13] | P_GFX_TXP[13] | M1  |
| N2  | P_GFX_RXN[13] | P_GFX_TXN[13] | M2  |
| M4  | P_GFX_RXP[14] | P_GFX_TXP[14] | K3  |
| M3  | P_GFX_RXN[14] | P_GFX_TXN[14] | K4  |
| K2  | P_GFX_RXP[15] | P_GFX_TXP[15] | J1  |
| K1  | P_GFX_RXN[15] | P_GFX_TXN[15] | J2  |

GRAPHICS

GPU

UMI

TRINITY-A8-SERIES\_BGA813

Delete GPU  
1202 Calvin

GPU

GLAN/Card reader  
WLAN

UMI

AG7 PCIE\_FTX\_DRX\_P0 CC33 1 2 .1U 0402 16V7K  
AG8 PCIE\_FTX\_DRX\_N0 CC34 1 2 .1U 0402 16V7K  
AE7 PCIE\_FTX\_DRX\_P1 CC35 1 2 .1U 0402 16V7K  
AE8 PCIE\_FTX\_DRX\_N1 CC36 1 2 .1U 0402 16V7K

AN6 UMI\_FTX\_MRX\_P0 CC37 1 2 .1U 0402 16V7K  
AM6 UMI\_FTX\_MRX\_N0 CC38 1 2 .1U 0402 16V7K  
AP6 UMI\_FTX\_MRX\_P1 CC39 1 2 .1U 0402 16V7K  
AB6 UMI\_FTX\_MRX\_N1 CC40 1 2 .1U 0402 16V7K  
AP4 UMI\_FTX\_MRX\_P2 CC41 1 2 .1U 0402 16V7K  
AR4 UMI\_FTX\_MRX\_N2 CC42 1 2 .1U 0402 16V7K  
AP3 UMI\_FTX\_MRX\_P3 CC43 1 2 .1U 0402 16V7K  
AR3 UMI\_FTX\_MRX\_N3 CC44 1 2 .1U 0402 16V7K

 P\_ZVSS W/S=8/12 mil, <3000mil

|  |            |                    |            |                          |                            |
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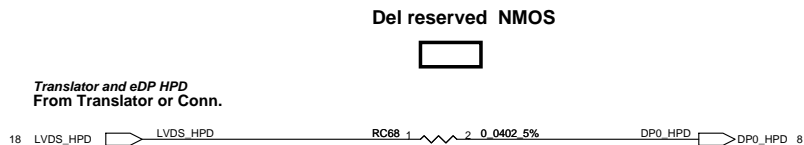








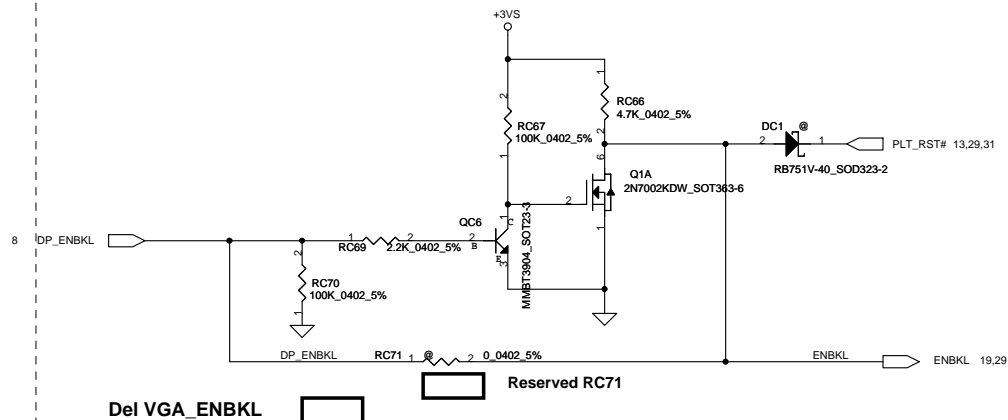
# HPD



Del reserved NMOS

12/06 Del FCH\_CRT\_HPD

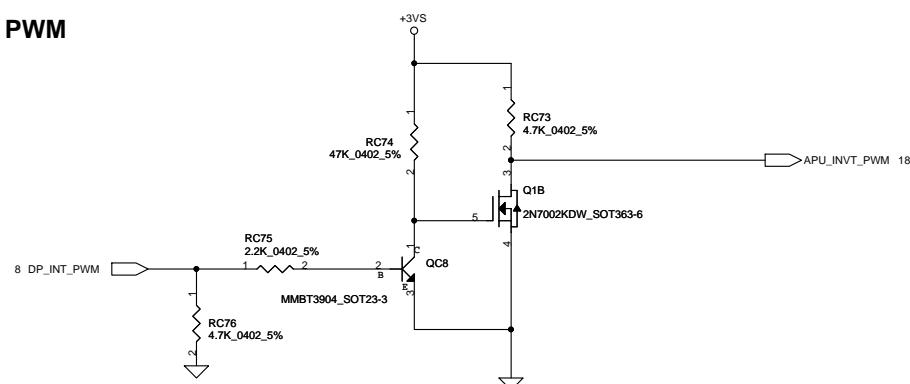
## Panel ENBKL



## eDP Panel ENVDD

Del eDP panel control

## Panel PWM



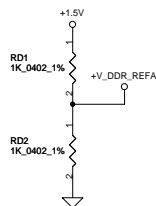
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+VREF\_DQ 15mil

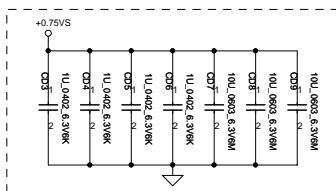
## DDR3 SO-DIMM A

All VREF traces should have 20 mil trace width

7 DDRA\_SDQ[0..63] DDRA\_SDQ[0..63]  
7 DDRA\_SDM[0..7] DDRA\_SDM[0..7]  
7 DDRA\_SMA[0..15] DDRA\_SMA[0..15]

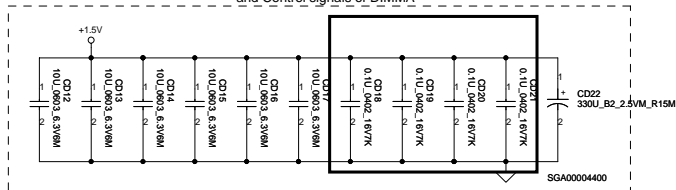


Layout Note:  
Place near JDIMM1.203 & JDIMM1.204

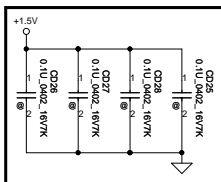


Layout Note:  
Place near JDIMM1

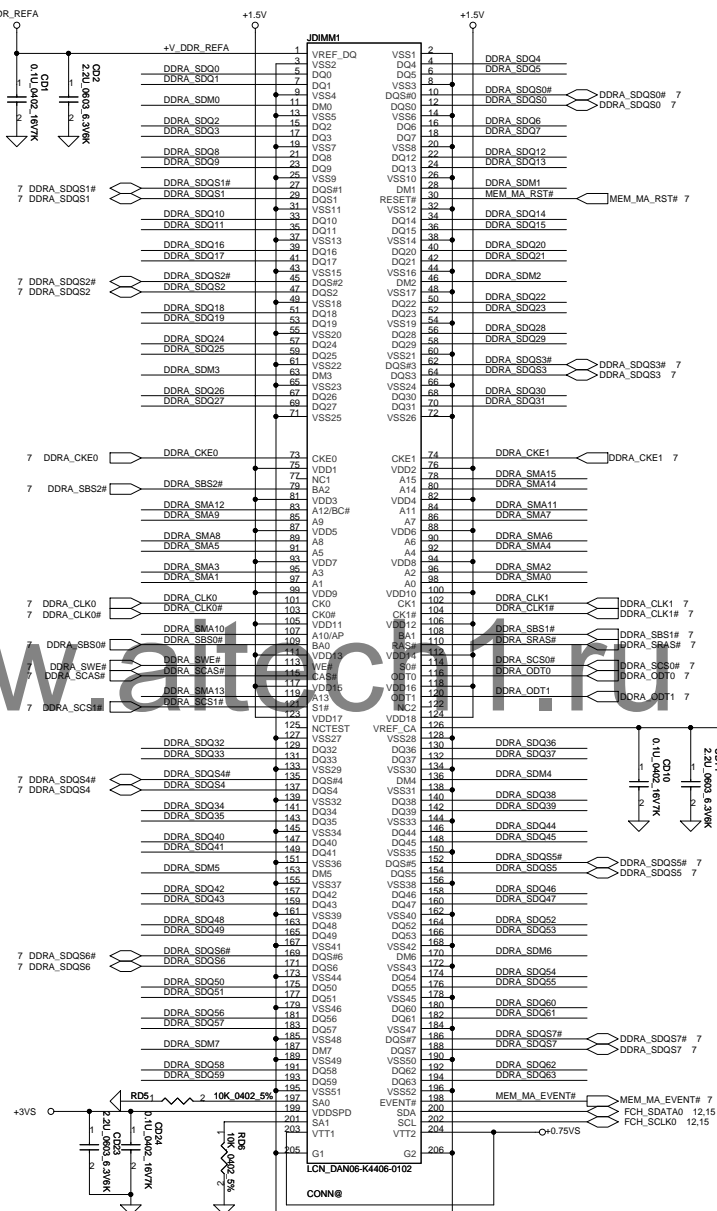
Layout Note: Place these 4 Caps near Command and Control signals of DIMMA



## DDR3 SO-DIMM A



SI# 8/16 Reserve 4 pcs 0.1uF for EMI noise issue

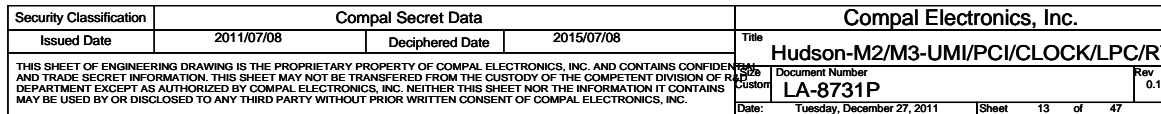


## DIMM\_A REV H:4mm

<Address: 00>

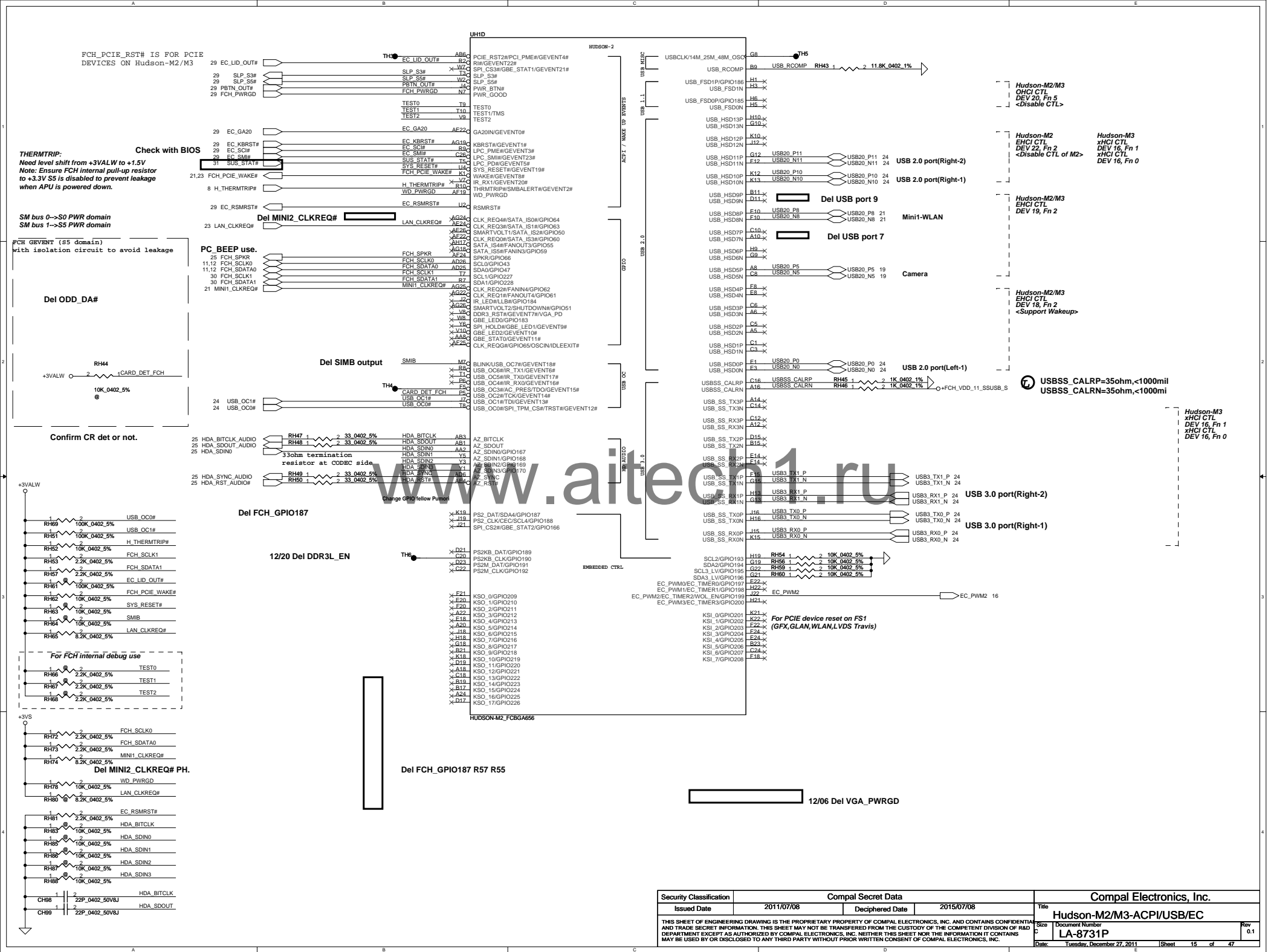
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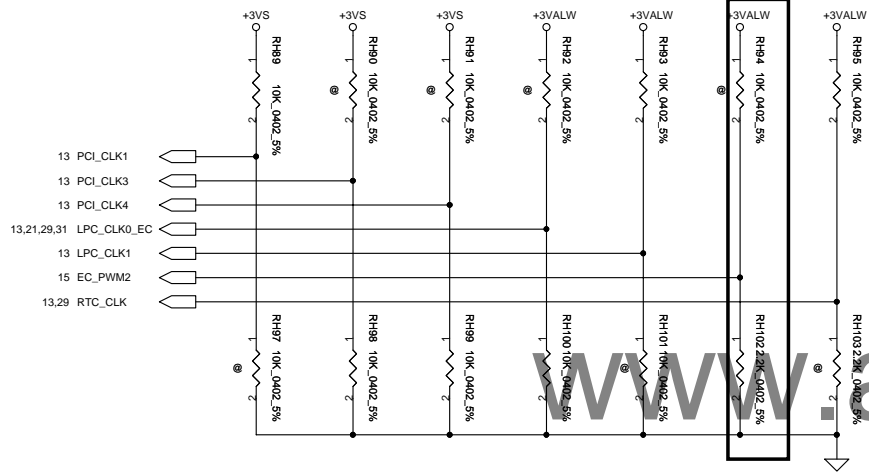




## STRAP PINS

Change to SPI

|           | PCI_CLK1                      | PCI_CLK3                            | PCI_CLK4                           | LPC_CLK0                  | LPC_CLK1                     | EC_PWM2            | RTC_CLK                                |
|-----------|-------------------------------|-------------------------------------|------------------------------------|---------------------------|------------------------------|--------------------|--|
| PULL HIGH | ALLOW<br>PCIE GEN2<br>DEFAULT | USE<br>DEBUG<br>STRAPS              | NON_FUSION<br>CLOCK MODE           | EC<br>ENABLED             | CLKGEN<br>ENABLED<br>DEFAULT | LPC ROM            | S5 PLUS<br>MODE<br>DISABLED<br>DEFAULT |
| PULL LOW  | FORCE<br>PCIE GEN1            | IGNORE<br>DEBUG<br>STRAP<br>DEFAULT | FUSION<br>CLOCK<br>MODE<br>DEFAULT | EC<br>DISABLED<br>DEFAULT | CLKGEN<br>DISABLE            | SPI ROM<br>DEFAULT | S5 PLUS<br>MODE<br>ENABLED             |



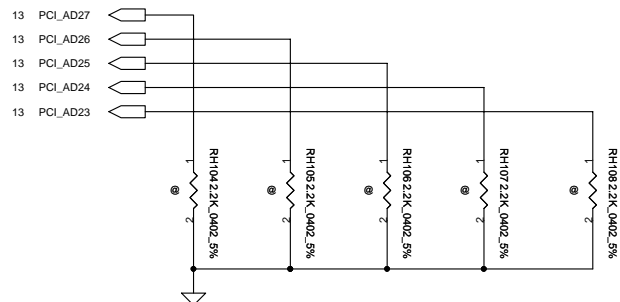
Remove VGA\_PD

Remove VGA\_PD

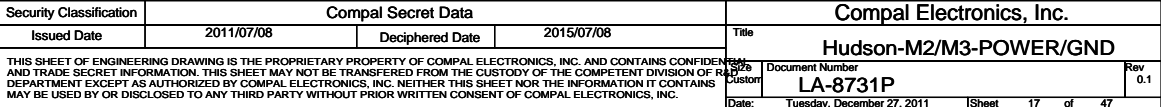
## DEBUG STRAPS

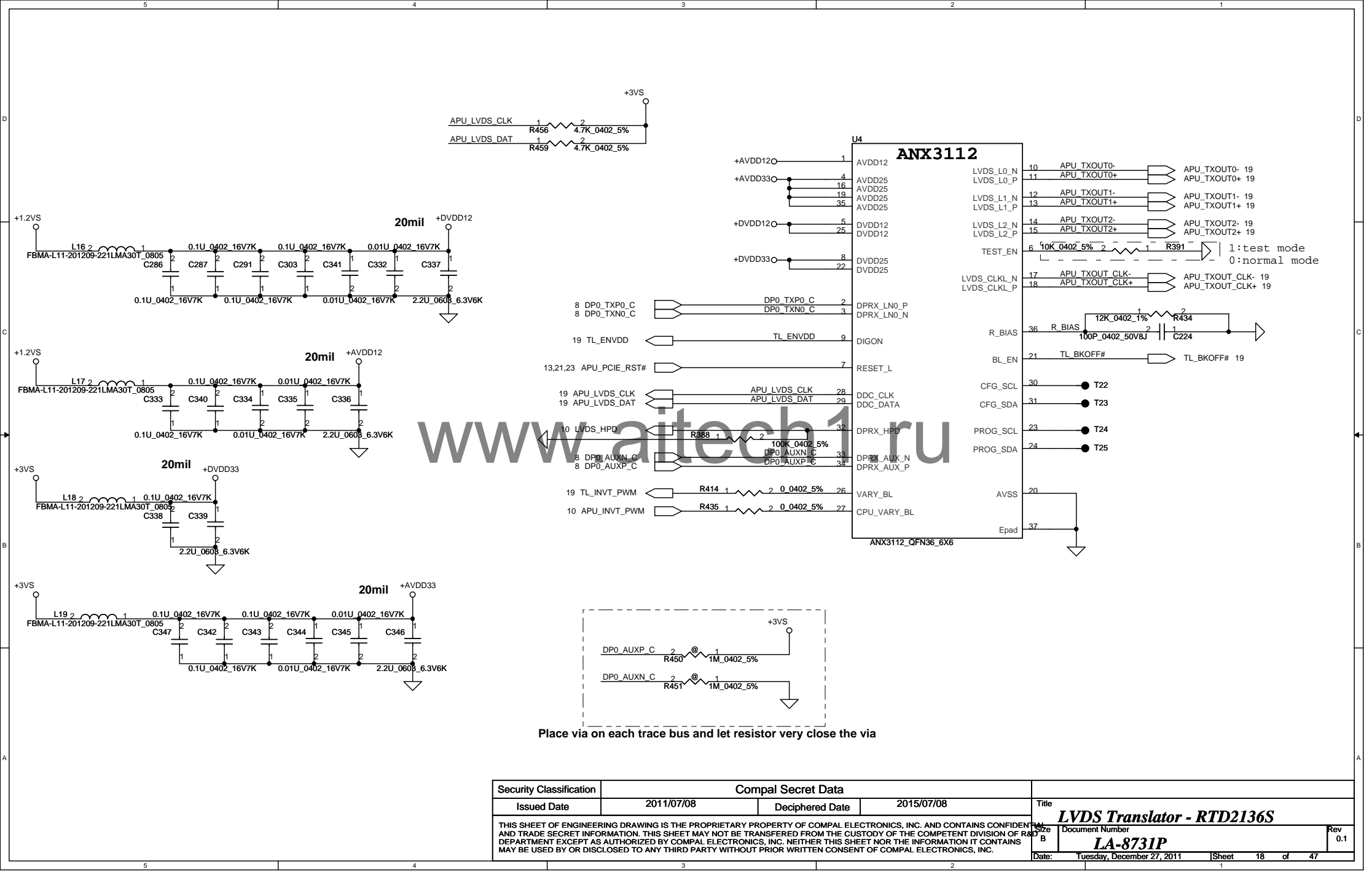
FCH HAS 15K INTERNAL PU FOR PCI\_AD[27:23]

|           | PCI_AD27                  | PCI_AD26                             | PCI_AD25                 | PCI_AD24                              | PCI_AD23                           |
|-----------|---------------------------|--------------------------------------|--------------------------|---------------------------------------|------------------------------------|
| PULL HIGH | USE PCI<br>PLL<br>DEFAULT | DISABLE<br>ILA<br>AUTORUN<br>DEFAULT | USE FC<br>PLL<br>DEFAULT | USE DEFAULT<br>PCIE STRAPS<br>DEFAULT | DISABLE PCI<br>MEM BOOT<br>DEFAULT |
| PULL LOW  | BYPASS<br>PCI PLL         | ENABLE<br>ILA<br>AUTORUN             | BYPASS<br>FC PLL         | USE EEPROM<br>PCIE STRAPS             | ENABLE PCI<br>MEM BOOT             |

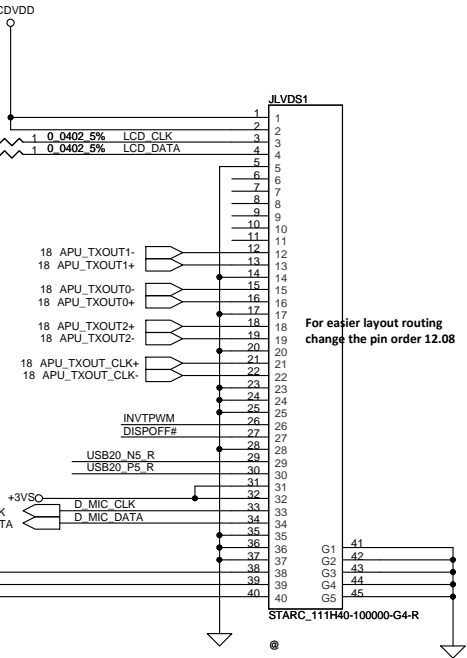
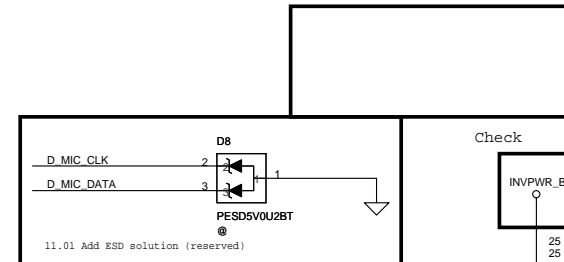
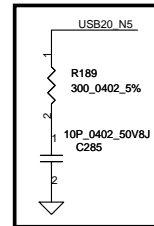
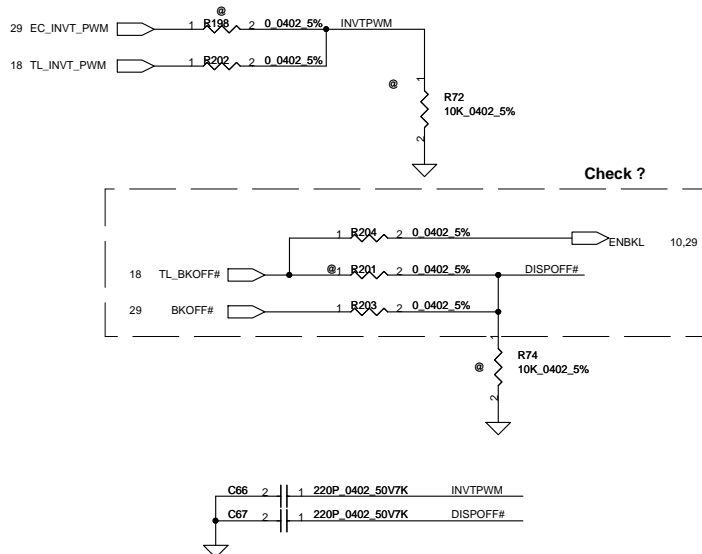
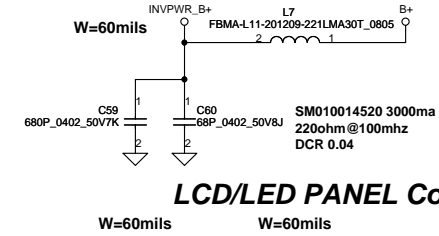
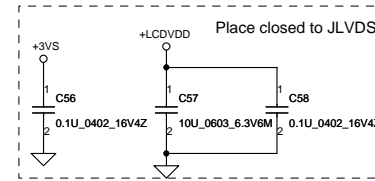


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| Customer   |                    |                 |                          | Document Number    |
| Date   |                    |                 |                          | LA-8731P           |
| Tuesday, December 27, 2011   |                    |                 |                          | Rev 0.1            |
| Sheet  |                    |                 |                          | 16 of 47           |

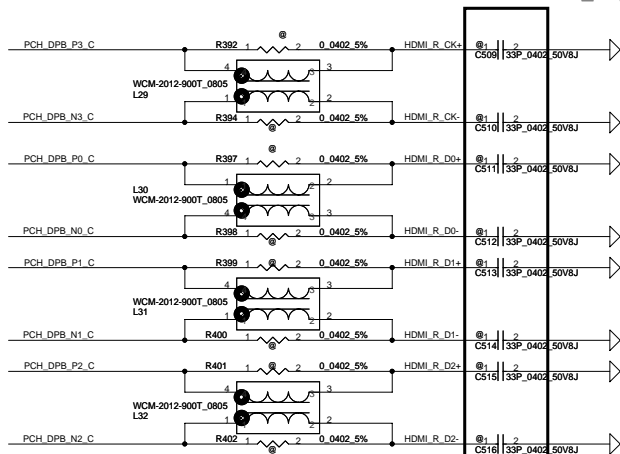
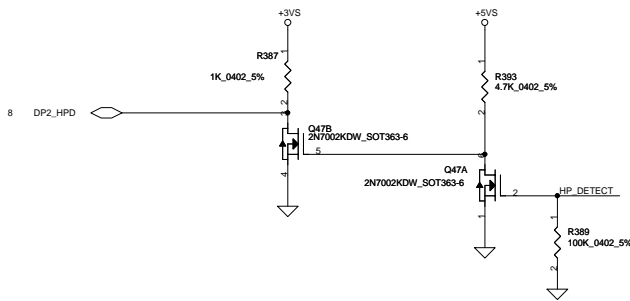
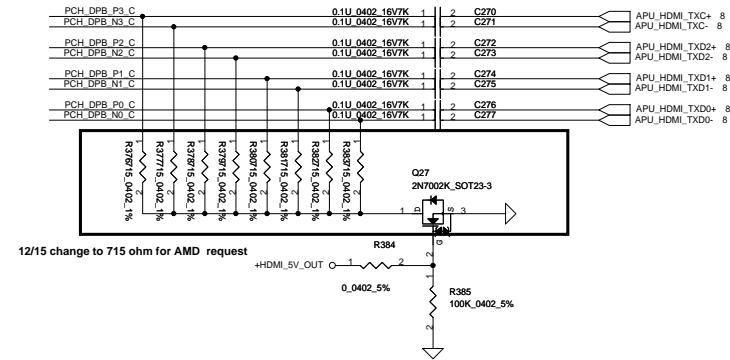




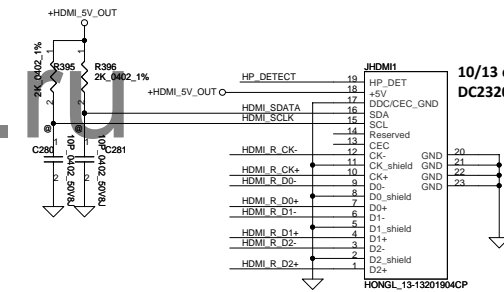
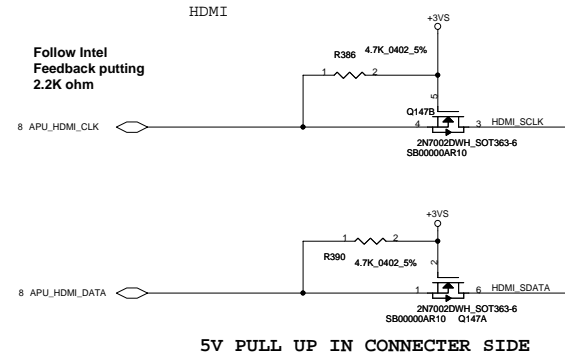
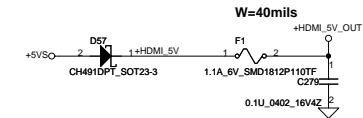


[illegible]

|   |                    |                 |            |                                |                 |       |
|---|--------------------|-----------------|------------|--------------------------------|-----------------|-------|
| Security Classification   | Compal Secret Data |                 |            | Compal Electronics, Inc.       |                 |       |
| Issued Date   | 2011/06/29         | Deciphered Date | 2011/06/29 | Title<br><b>LVDS Connector</b> |                 |       |
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|   |                    |                 |            |                                | <b>LA-8731P</b> | 0.1   |
| Date: Tuesday, December 27, 2011  |                    |                 |            | Sheet                          | 19              | of 47 |

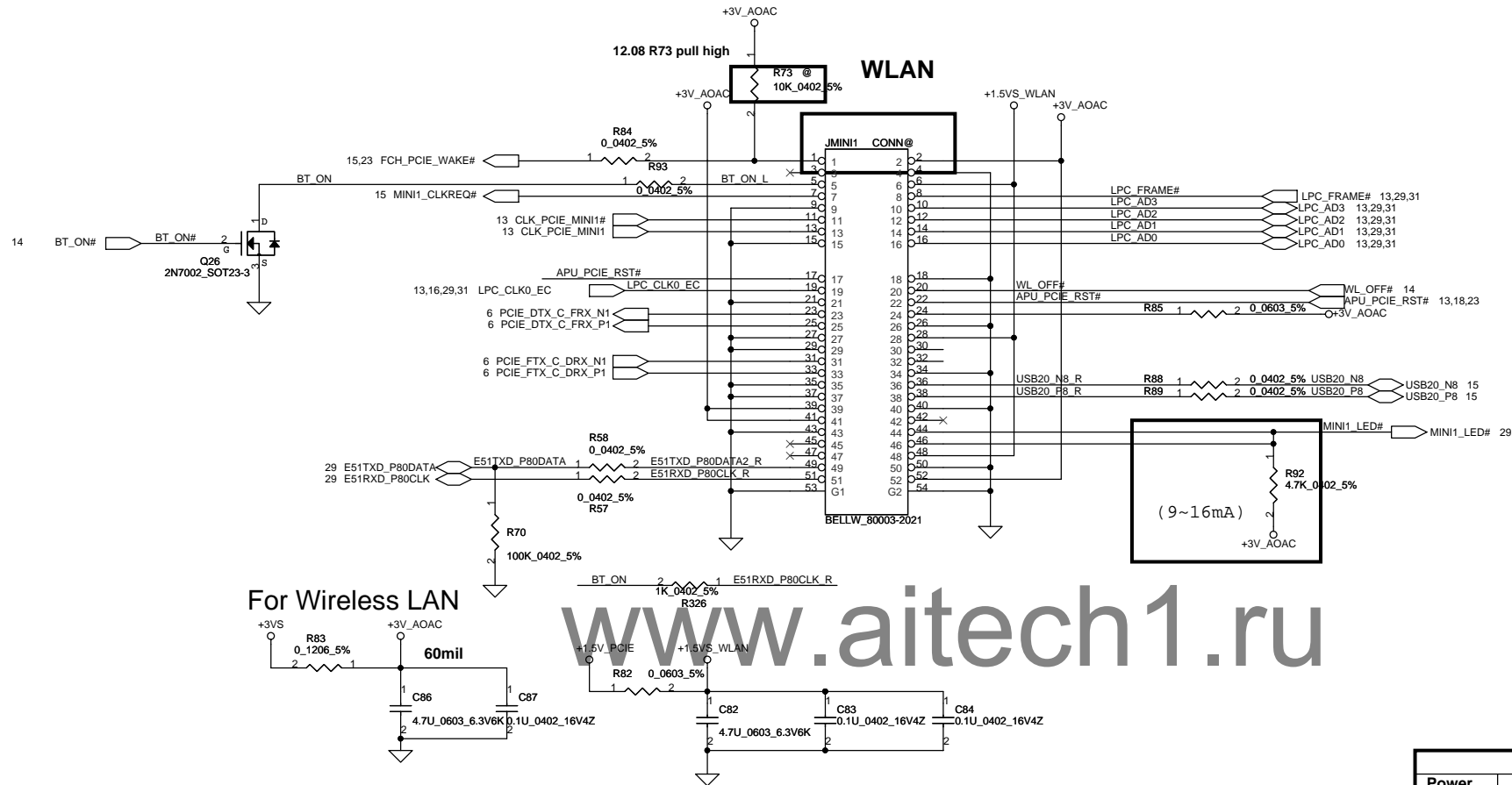


Follow EMI request add 33pF cap to GND.  
11.02

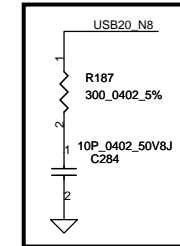


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|   |            |                    |            |                          |                 |
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| Security Classification   |            | Compal Secret Data |            | Compal Electronics, Inc. |                 |
| Issued Date   | 2011/06/29 | Deciphered Date    | 2011/06/29 | Title                    | HDMI Conn       |
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|   |            |                    |            | Date                     | LA-8731P        |
|   |            |                    |            | Sheet                    | 20 of 47        |
|   |            |                    |            | Rev                      | 0.1             |



12/21 for AMD issue workaround



| Mini Card Power Rating |                    |        |                      |
|------------------------|--------------------|--------|----------------------|
| Power                  | Primary Power (mA) |        | Auxiliary Power (mA) |
|                        | Peak               | Normal |                      |
| +3VS                   | 1000               | 750    | Normal               |
| +3V                    | 330                | 250    | 250 (wake enable)    |
| +1.5VS                 | 500                | 375    | 5 (Not wake enable)  |

11/23 Del AOAC

|   |            |                    |            |                 |          |
|---|------------|--------------------|------------|-----------------|----------|
| Security Classification   |            | Compal Secret Data |            | Title           |          |
| Issued Date   | 2011/06/29 | Deciphered Date    | 2011/06/29 | Document Number | Rev      |
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| Date: Tuesday, December 27, 2011  |            |                    |            | Sheet           | 21 of 47 |

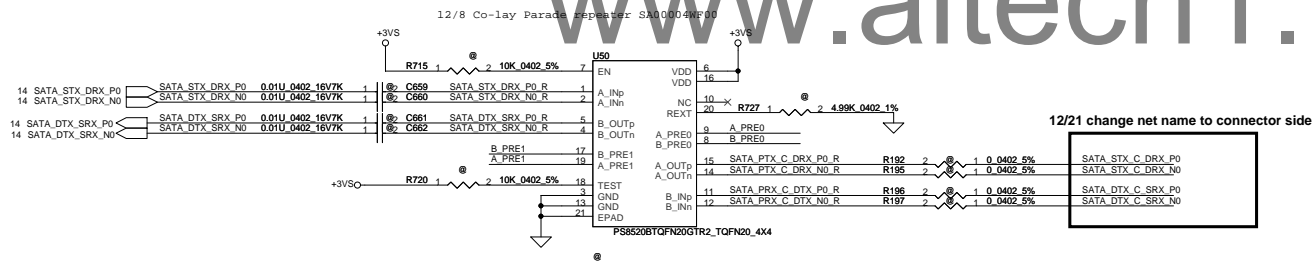
Compal Electronics, Inc.

MiniCard & Wlan

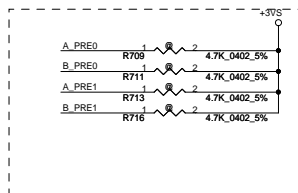
# mSATA Conn.

12/12 Del mSATA by customer

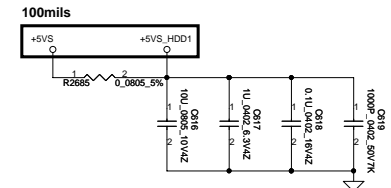
## SATA Redriver



Note: Add EQ pin for STA1102RQTR



SATA connector



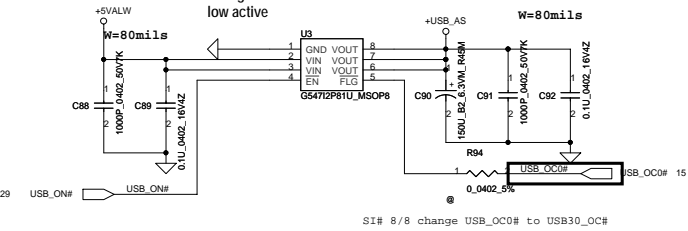
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| Issued Date   | 2011/06/29 | Deciphered Date    | 2011/06/29 | Title                    | mSATA Connector            |
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|   |            |                    |            | Date                     | Tuesday, December 27, 2011 |
|   |            |                    |            | Sheet                    | 22 of 47                   |

|   |                           |                 |                 |                                |
|---|---------------------------|-----------------|-----------------|--------------------------------|
| Security Classification   | Compal Secret Data        |                 | Title           |                                |
| Issued Date   | 2011/06/29                | Deciphered Date | 2011/0/03       | LAN&CardReader Realtek RTL8411 |
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| Date  | Yamada, December 27, 2011 | Issue           | 23              | of 47                          |

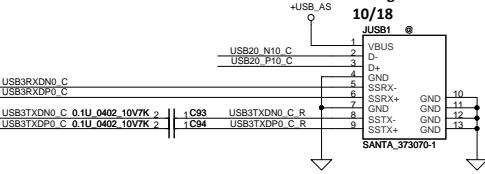


## USB3.0

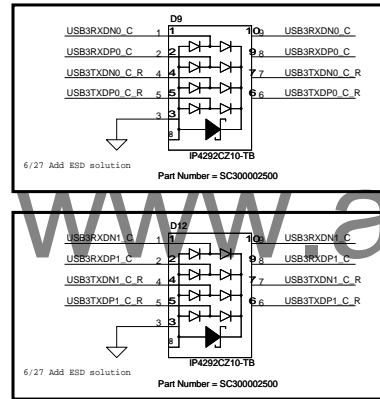
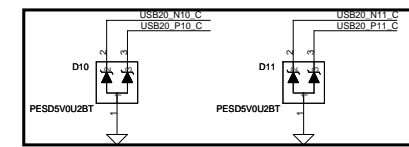
USB3.0 need support 2.5A  
change USB PWR SW SA00003TV00  
low active



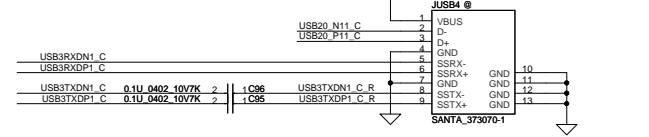
Change conn to SANTA-373070



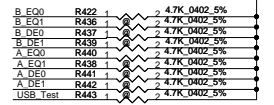
Change P/N from SCA00000T00 to SCA00001L00



Change conn to SANTA-373070



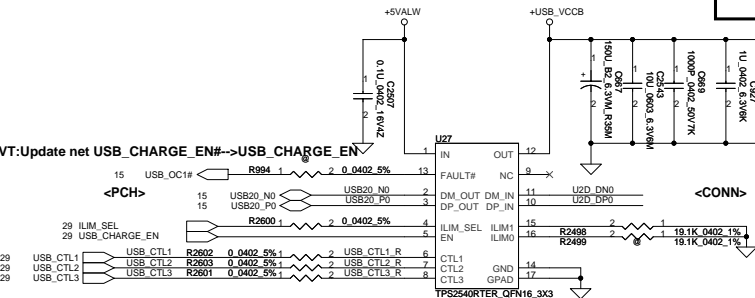
Programable output pre-emphasis level setting for channel A1&A2, B1&B2  
3.3V tolerant. Internally pulled down at ~150KΩ  
[A\_DE1, A\_DE0] [B\_DE1, B\_DE0] == ==  
LL: 3.5dB de-emphasis  
LH: No de-emphasis  
HL: 2.7dB de-emphasis  
HH: 5.0dB de-emphasis



## USB2.0 & charger

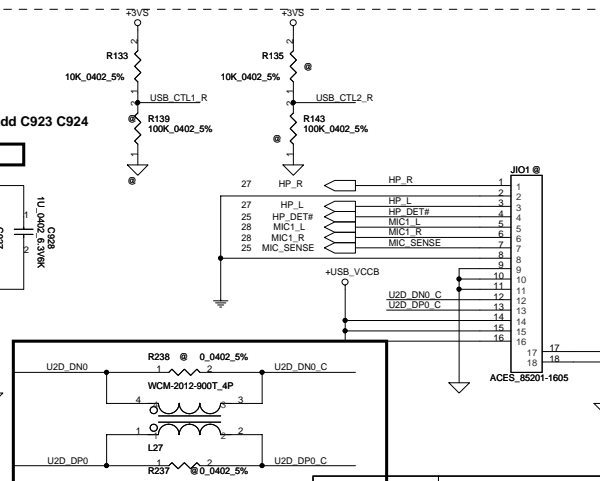
USB charger footprint need change to TPS2543  
TPS2543 : SA000059H00 pin 9 (Status); 2540 pin9 (NC)

Pre MP:Add C923 C924

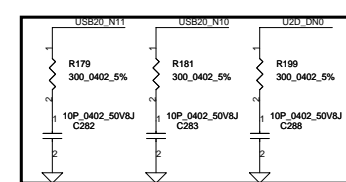


PVT:Remove R2664 R2499 R2500 R2501 for DFX issue

Follow EMI request add choke  
11.08



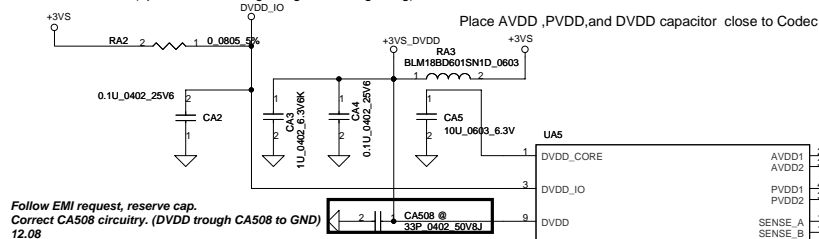
12/21 for AMD issue workaround



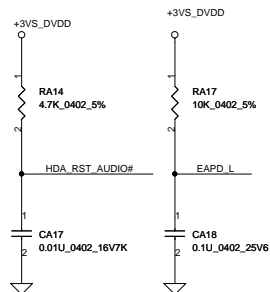
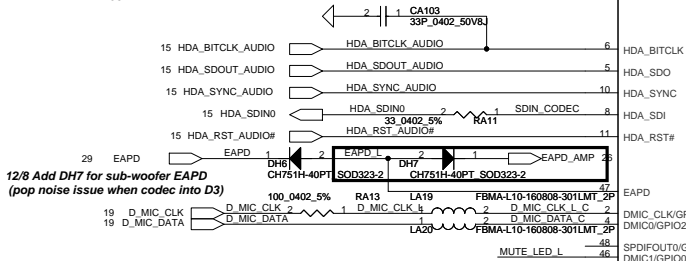
Check mode with customer?

| State       | S0   |      |      | S3, S4, S5 |      |      |
|-------------|------|------|------|------------|------|------|
| Mode        | CDP  |      |      | DCP        |      |      |
| Control pin | CTL1 | CTL2 | CTL3 | ILIM_SEL   | CTL1 | CTL2 |
|             | 1    | 1    | 1    | 1          | 0    | 0    |

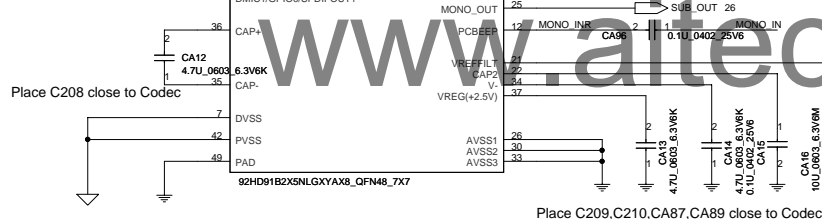
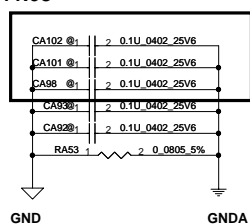
DVDD\_IO should match with HDA Bus level(optional for 3.3V signaling or 1.5V signaling)



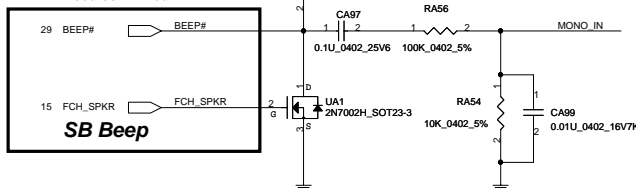
Follow EMI request, reserve cap.  
Correct CA508 circuitry. (DVDD trough CA508 to GND)  
12.08



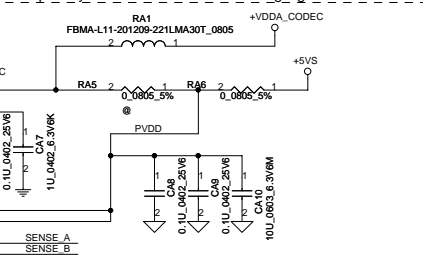
Follow EMI request, reserve cap.  
11.03



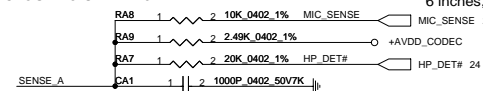
Need confirmed.



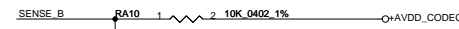
Notes:  
Keep PVDD supply and speaker traces routed on the DGND plane.  
Keep away from AGND and other analog signals



PLACE CLOSE TO U1 PIN 13



If Sense\_A total length is greater than 6 inches, change C12 to 0.1uF



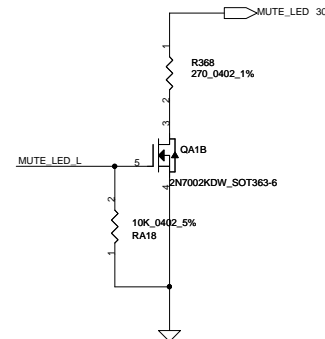
PLACE CLOSE TO U1 PIN 14

If Sense\_B is un-used, then pull high Sense\_B to AVDD by 10Kohm resistor

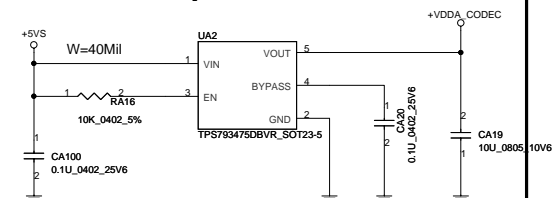
HP Jack

Ext MIC

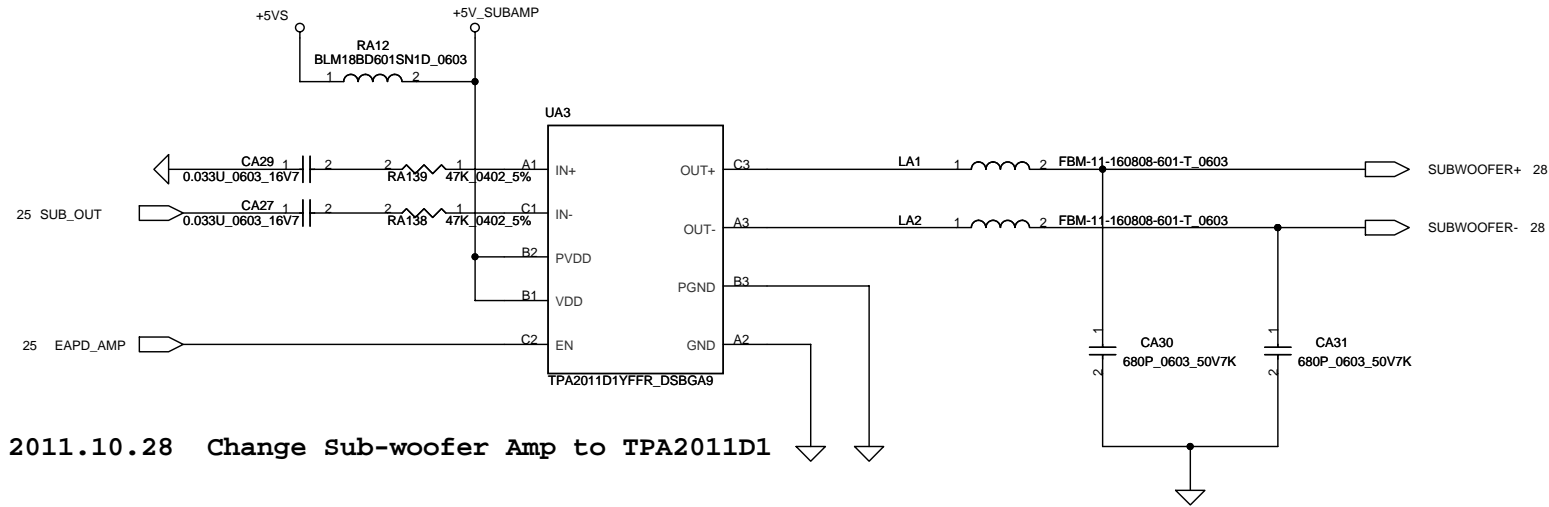
Internal SPKR(front stereo speaker)



9/27 LDO TPS793475DBVR for audio power



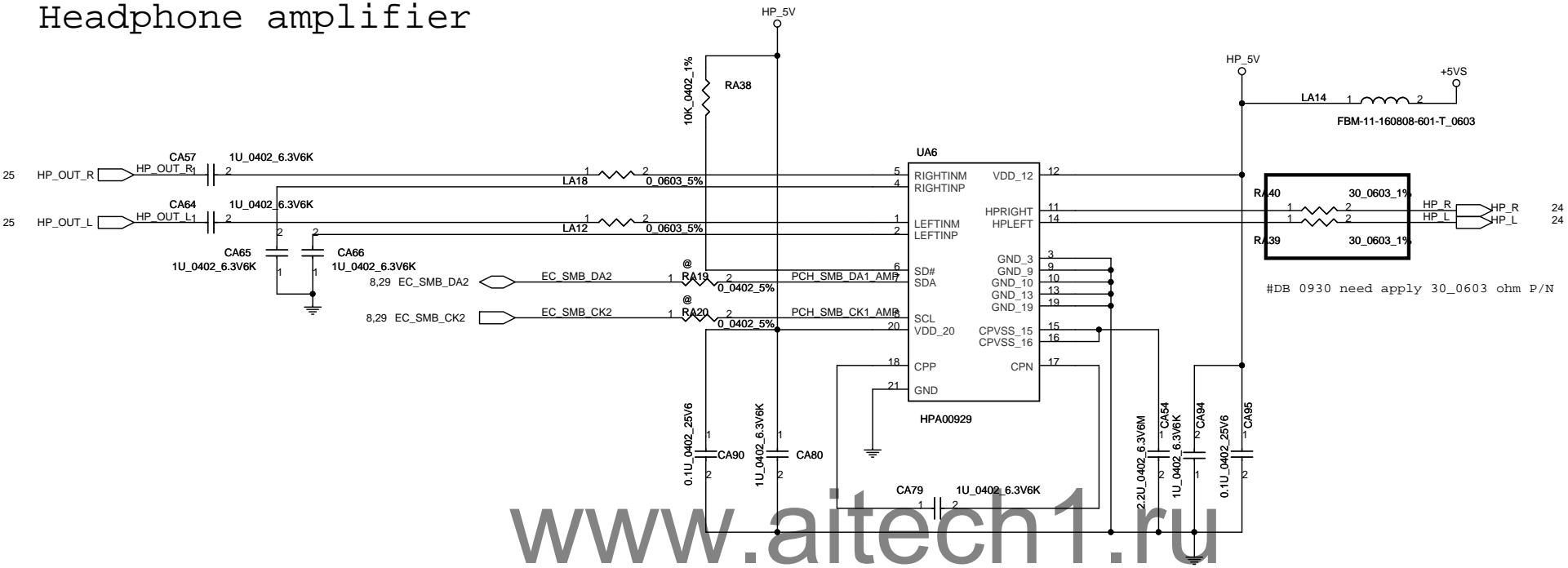
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|   |            | Date               |            | Tuesday, December 27, 2011 | 0.1 |
|   |            | Sheet              |            | 25                         | 47  |



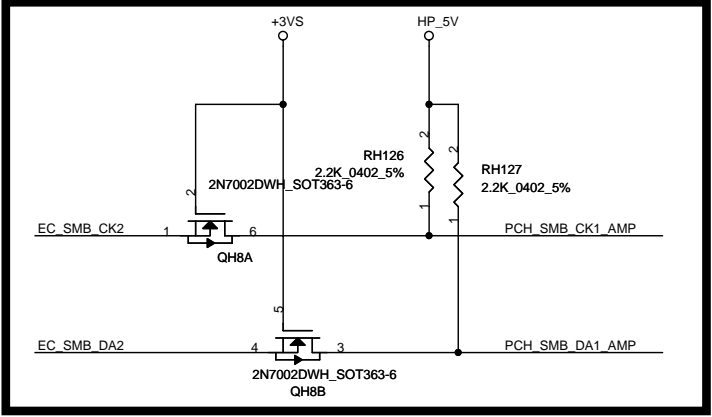
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|   |            |                    |            |                          |                            |
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|   |            |                    |            | B                        | 0.1                        |
|   |            |                    |            | Date:                    | Tuesday, December 27, 2011 |
|   |            |                    |            | Sheet                    | 26 of 47                   |

Headphone amplifier

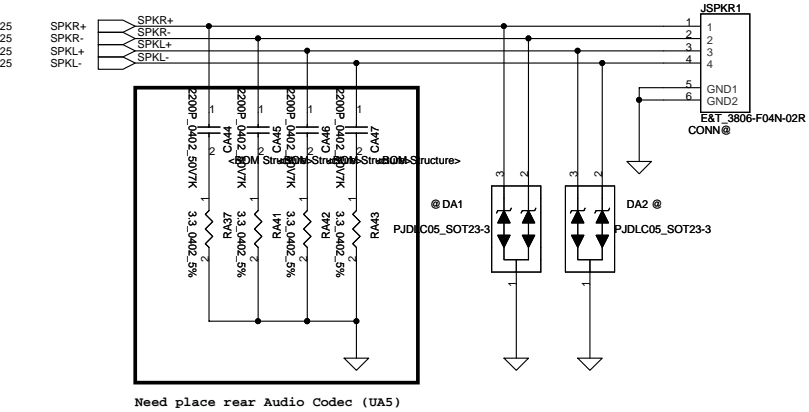


Add level shift 11.06

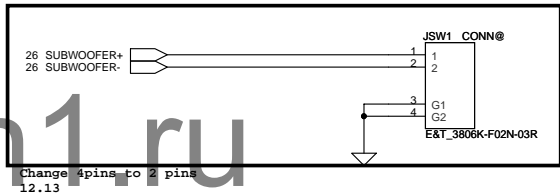
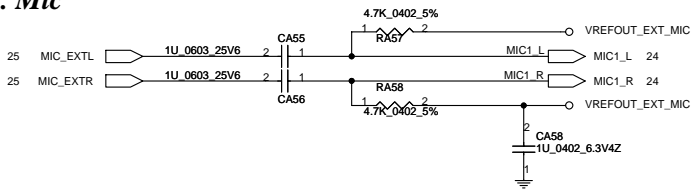


|   |            |                    |            |                          |                            |
|---|------------|--------------------|------------|--------------------------|----------------------------|
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|   |            |                    |            | Rev                      | 0.1                        |
|   |            |                    |            | Date:                    | Tuesday, December 27, 2011 |
|   |            |                    |            | Sheet                    | 27 of 47                   |

Front Speaker Connector 1

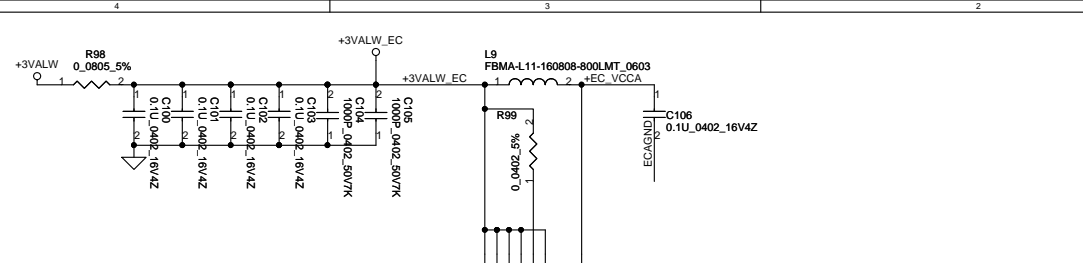


Ext. Mic



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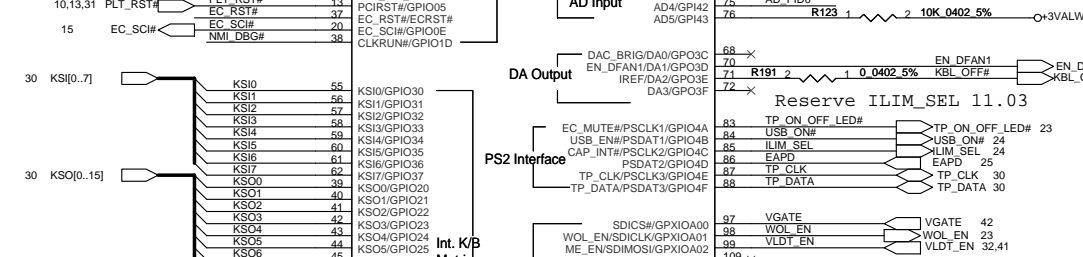
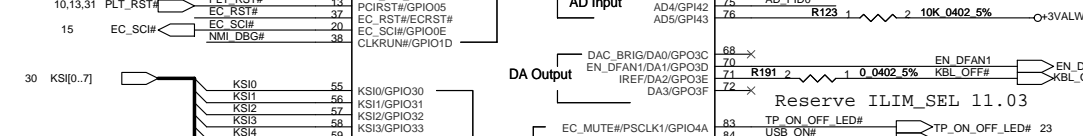
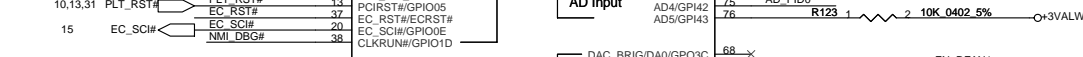
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| Security Classification   |  | Compal Secret Data         |  | Compal Electronics, Inc. |  |
| Issued Date   |  | Deciphered Date            |  | Title                    |  |
| 2009/04/07  |  | 2012/10/21                 |  | Audio SPK Conn/Jack/MIC  |  |
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|   |  | Custom                     |  | LA-8731P                 |  |
| Date:   |  | Tuesday, December 27, 2011 |  | Sheet 28 of 47           |  |
|   |  |                            |  | Rev 0.1                  |  |



Pin 15 to 27 connection diagram for the LPC1114. The diagram shows the following connections:

- Pin 15: EC\_GA20 to EC\_GA20 (1), EC\_KBRST# to EC\_KBRST# (2)
- Pin 16: EC\_KBRST# to EC\_KBRST# (2)
- Pin 17: SERIRQ to SERIRQ (3)
- Pin 18: SERIRQ to SERIRQ (3)
- Pin 19: LPC\_FRAME# to LPC\_FRAME# (4)
- Pin 20: LPC\_FRAME# to LPC\_FRAME# (4)
- Pin 21: LPC\_AD3 to LPC\_AD3 (5)
- Pin 22: LPC\_AD3 to LPC\_AD3 (5)
- Pin 23: GATEA20/GPIO0 to GATEA20/GPIO0 (1)
- Pin 24: KBRST#/GPIO1 to KBRST#/GPIO1 (2)
- Pin 25: SERIRQ# to SERIRQ# (3)
- Pin 26: FAN\_PWM1/GPIO10 to FAN\_PWM1/GPIO10 (10)
- Pin 27: LPC\_FRAME#/LFRAME# to LPC\_FRAME#/LFRAME# (4)
- Pin 28: LPC\_AD3 to LPC\_AD3 (5)
- Pin 29: AC0FF/FAN\_PWM1/GPIO13 to AC0FF/FAN\_PWM1/GPIO13 (13)
- Pin 30: AC\_LED# to AC\_LED# (21)
- Pin 31: BEEP# to BEEP# (23)
- Pin 32: T28 to T28 (27)

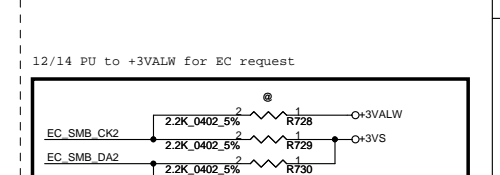
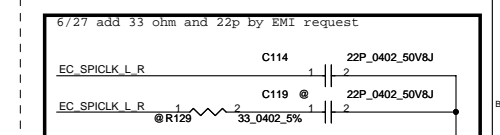
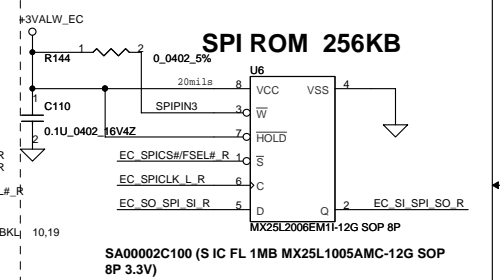
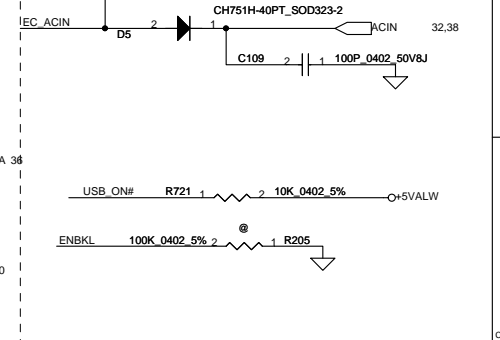
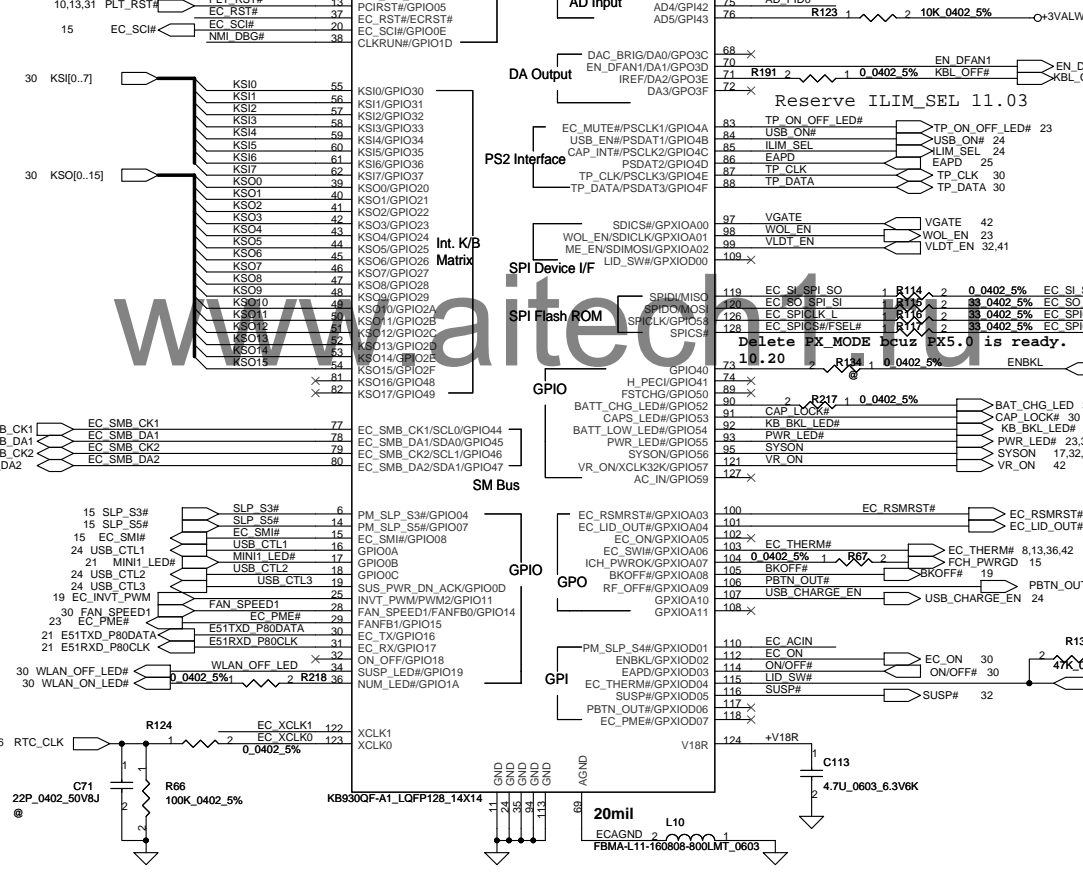
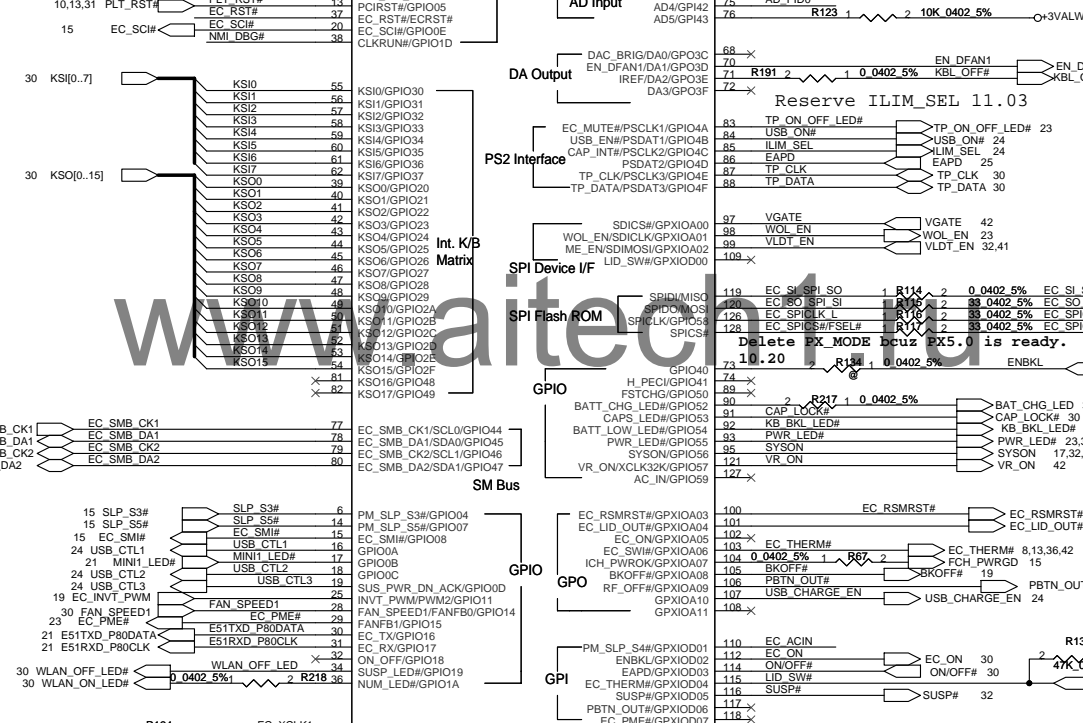
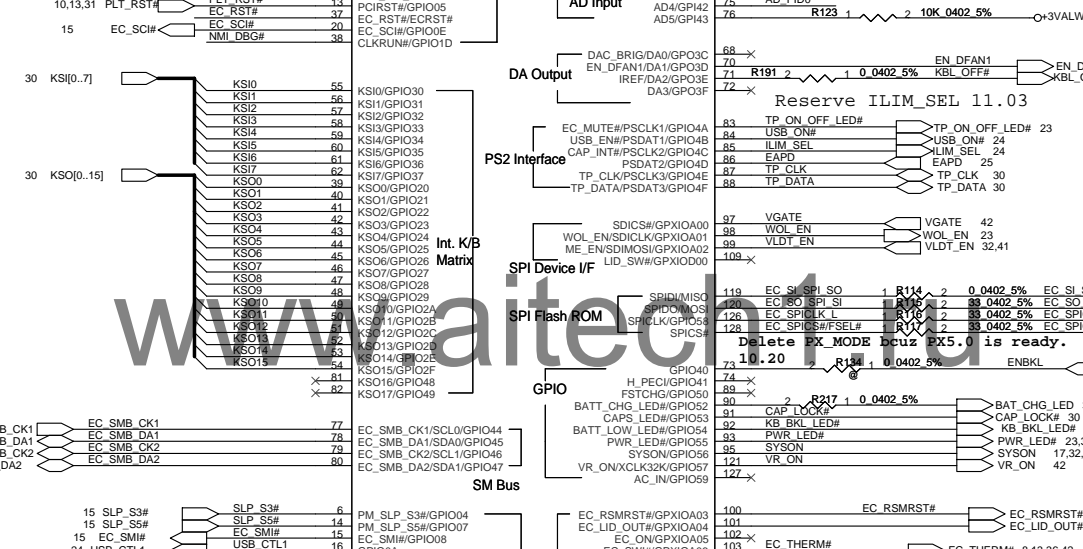
Power pins are indicated as VCC and AVCC.



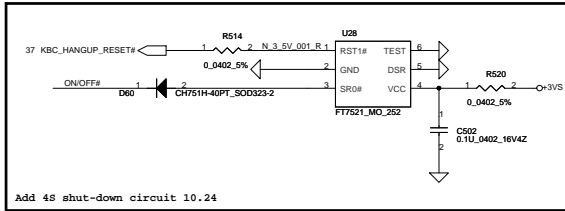
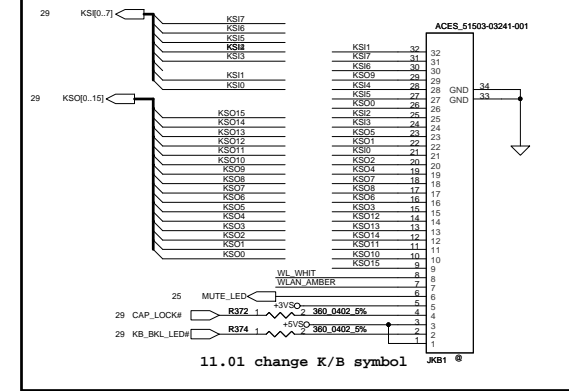
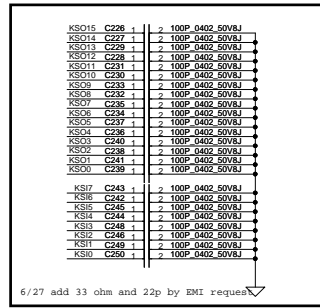
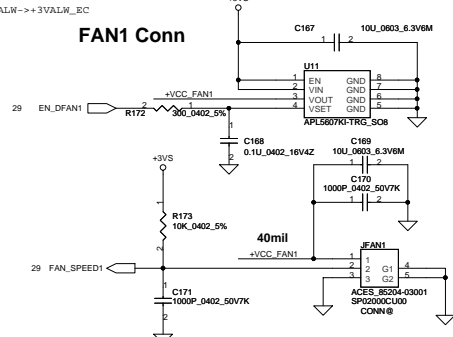
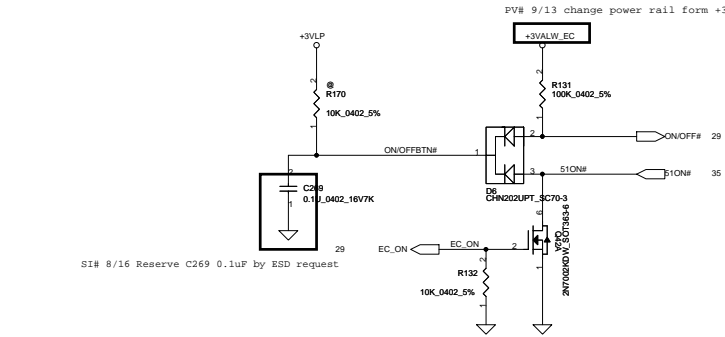
10,13,15 PLT\_RST# EC\_RST# 14 PCIRST#/GPIO05 EC\_RST#/ECRST# 14 AD/PG142 AD/PG143 AD/PG144 76 R123 2 10K 0.402 5% +3.3VALL

15 EC\_SCJ# EC\_SCW#/GPIO06 CLKRUN#/GPIO1D 38

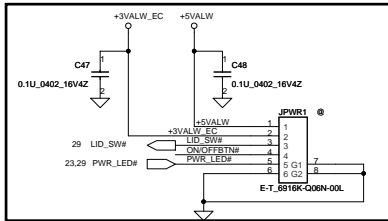
30 KSJ[0..7] KSJ0 56 KSJ0/GPIO30 KSJ1/GPIO31 KSJ2/GPIO32 KSJ3/GPIO33 KSJ4/GPIO34 KSJ5/GPIO35 KSJ6/GPIO36 KSJ7/GPIO37 KSJ8/GPIO38 KSJ9/GPIO39 KSJ10/GPIO40 KSJ11/GPIO41 KSJ12/GPIO42 KSJ13/GPIO43 KSJ14/GPIO44 KSJ15/GPIO45 KSJ16/GPIO46 KSJ17/GPIO47 KSJ18/GPIO48 KSJ19/GPIO49 KSJ20/GPIO50 KSJ21/GPIO51 KSJ22/GPIO52 KSJ23/GPIO53 KSJ24/GPIO54 KSJ25/GPIO55 KSJ26/GPIO56 KSJ27/GPIO57 KSJ28/GPIO58 KSJ29/GPIO59 KSJ30/GPIO60 KSJ31/GPIO61 KSJ32/GPIO62 KSJ33/GPIO63 KSJ34/GPIO64 KSJ35/GPIO65 KSJ36/GPIO66 KSJ37/GPIO67 KSJ38/GPIO68 KSJ39/GPIO69 KSJ40/GPIO70 KSJ41/GPIO71 KSJ42/GPIO72 KSJ43/GPIO73 KSJ44/GPIO74 KSJ45/GPIO75 KSJ46/GPIO76 KSJ47/GPIO77 KSJ48/GPIO78 KSJ49/GPIO79 KSJ50/GPIO80 KSJ51/GPIO81 KSJ52/GPIO82 KSJ53/GPIO83 KSJ54/GPIO84 KSJ55/GPIO85 KSJ56/GPIO86 KSJ57/GPIO87 KSJ58/GPIO88 KSJ59/GPIO89 KSJ60/GPIO90 KSJ61/GPIO91 KSJ62/GPIO92 KSJ63/GPIO93 KSJ64/GPIO94 KSJ65/GPIO95 KSJ66/GPIO96 KSJ67/GPIO97 KSJ68/GPIO98 KSJ69/GPIO99 KSJ70/GPIO100 KSJ71/GPIO101 KSJ72/GPIO102 KSJ73/GPIO103 KSJ74/GPIO104 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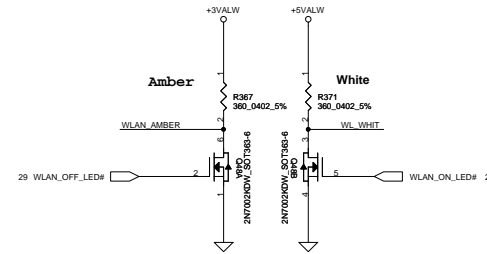


12/8 update JFWR1 symbol

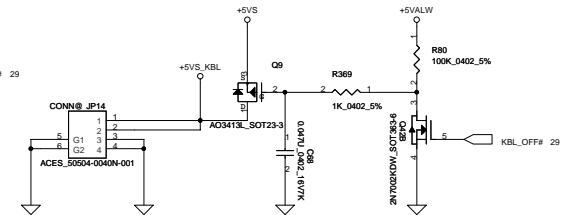


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TP/B TO M/B



Keyboard backlight Conn



TP/B TO M/B

TP/B TO M/B

TP/B TO M/B

TP/B TO M/B

TP/B TO M/B

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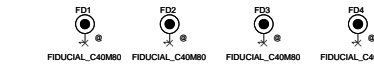
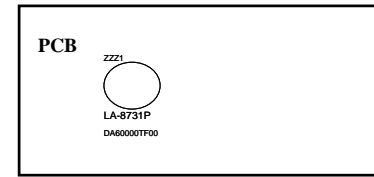
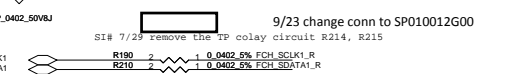
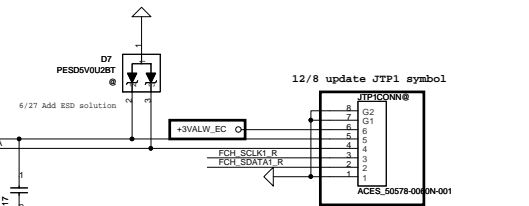
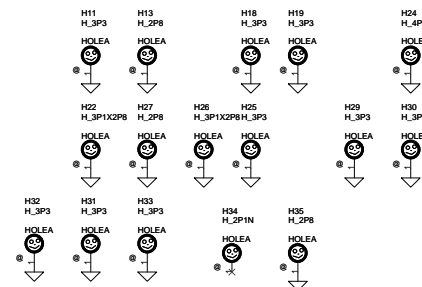
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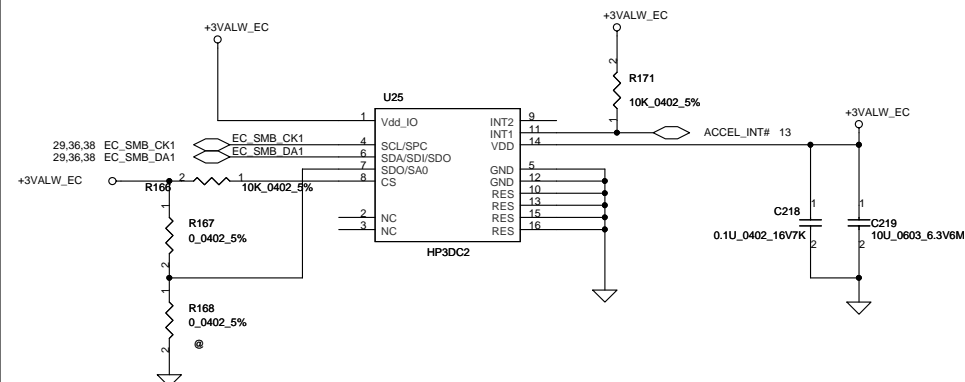
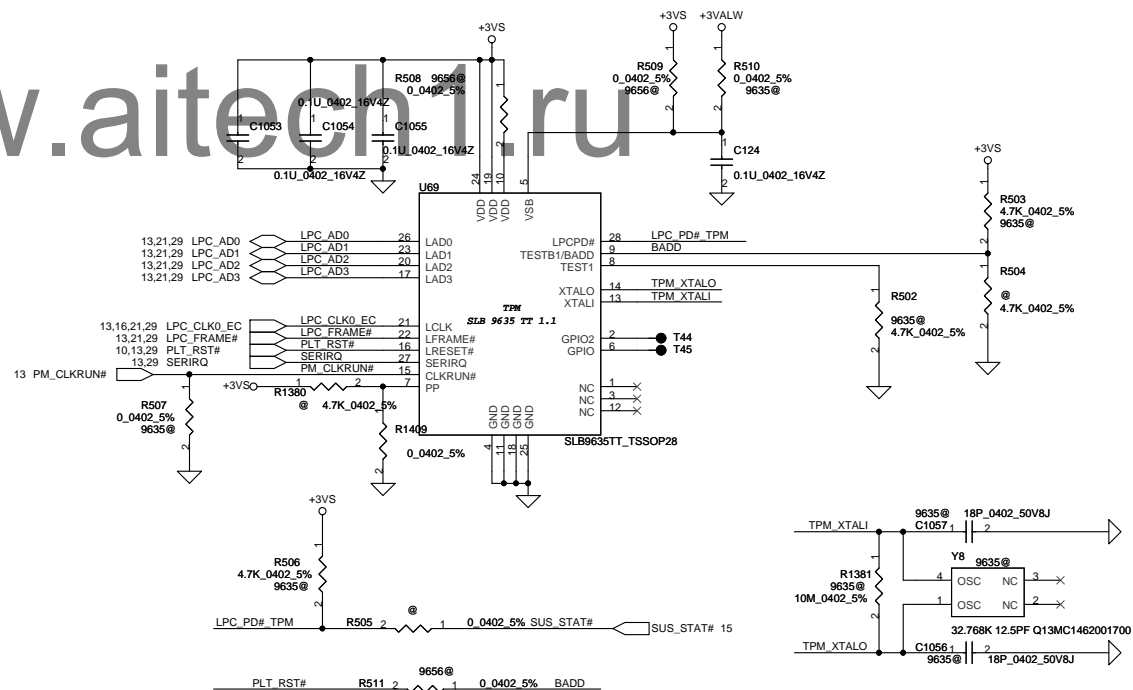
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|   |                    |                 |                          | Date: Tuesday, December 27, 2011 |
|   |                    |                 |                          | Sheet 30 of 47                   |

***ACCELEROMETER Address: 0x50/0x52***

***TPM1.2***

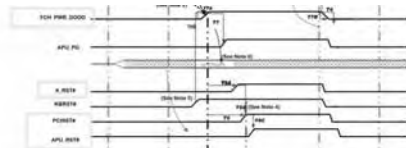
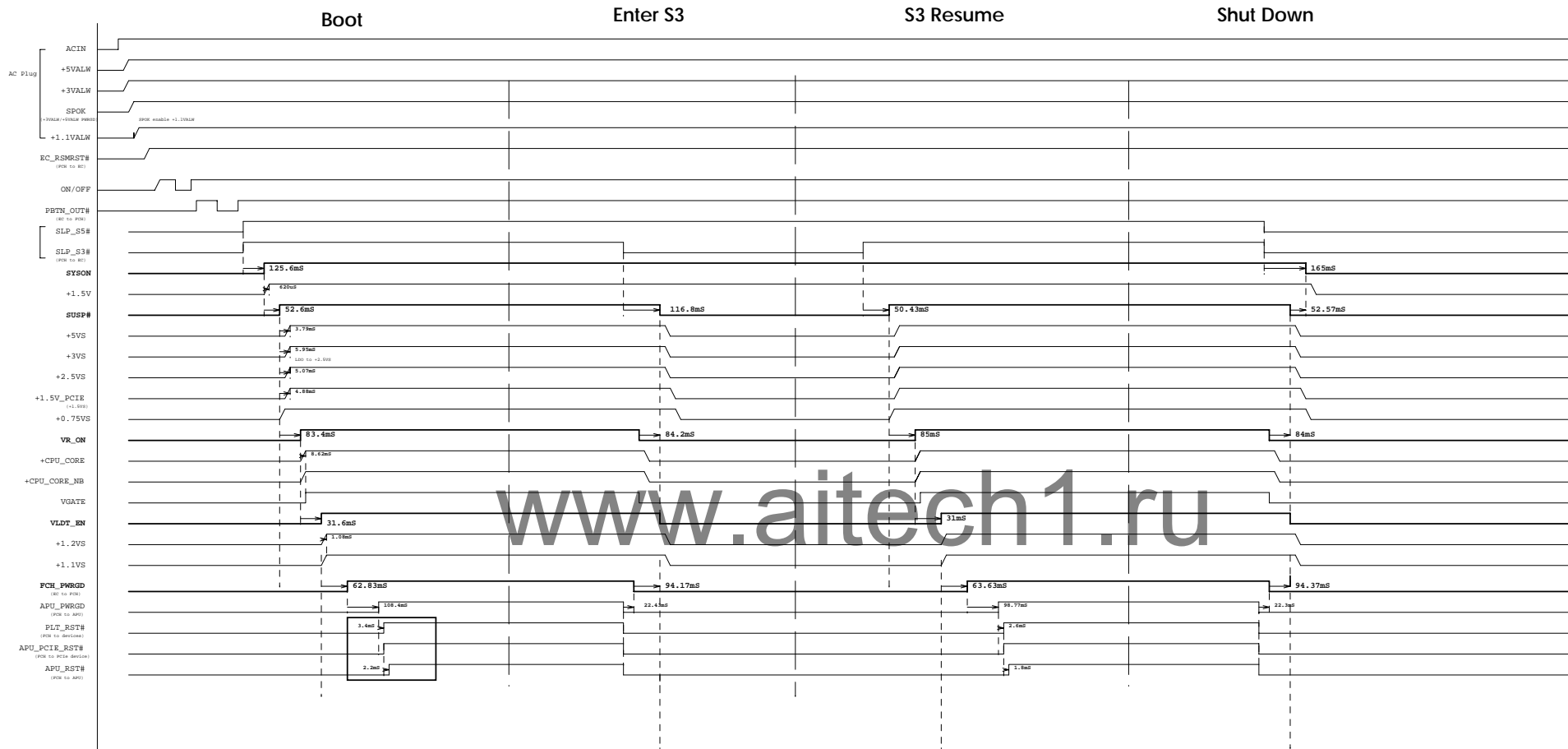
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|  |                            |                    |            | Document Number          | 0.1         |
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| Date:  | Tuesday, December 27, 2011 | Sheet              | 31         | of                       | 47          |

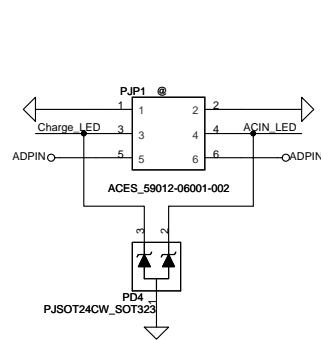




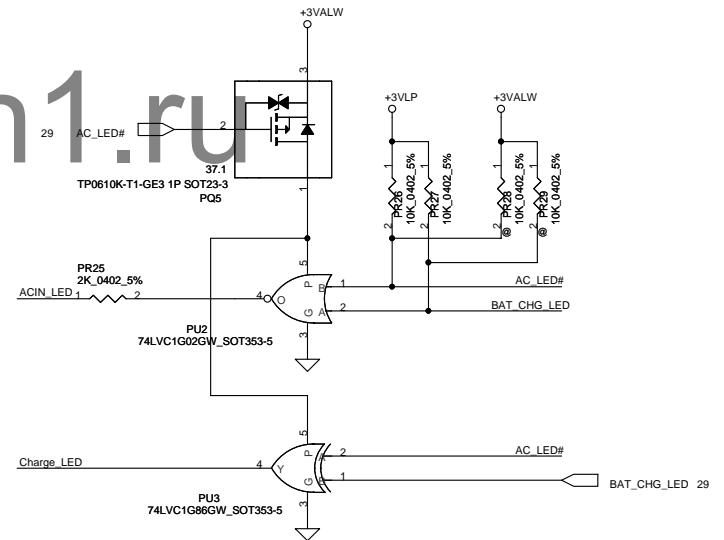
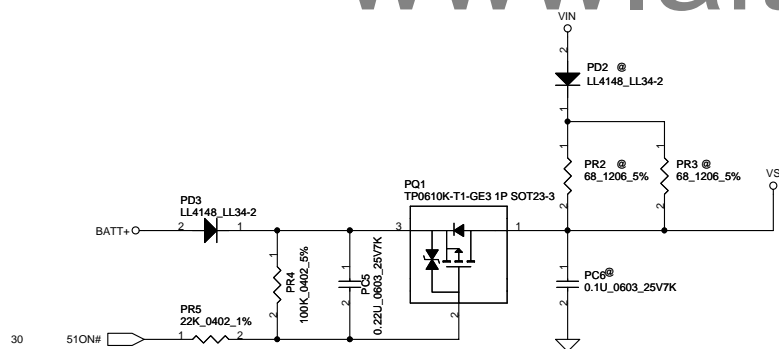
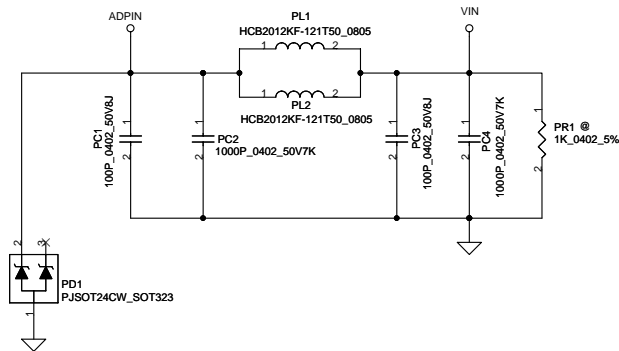
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|   |                    |                 |            | Date:                    | Tuesday, December 27, 2011 | Sheet 33 of 47 |

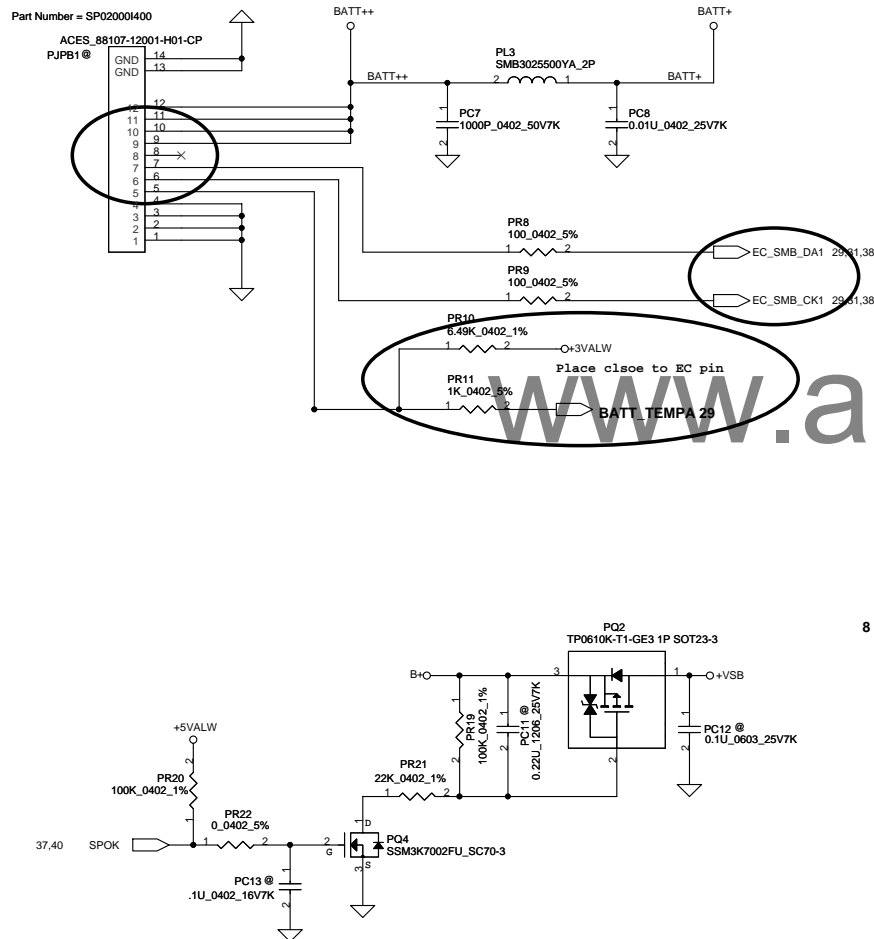




ESD diode : SCA00001G00

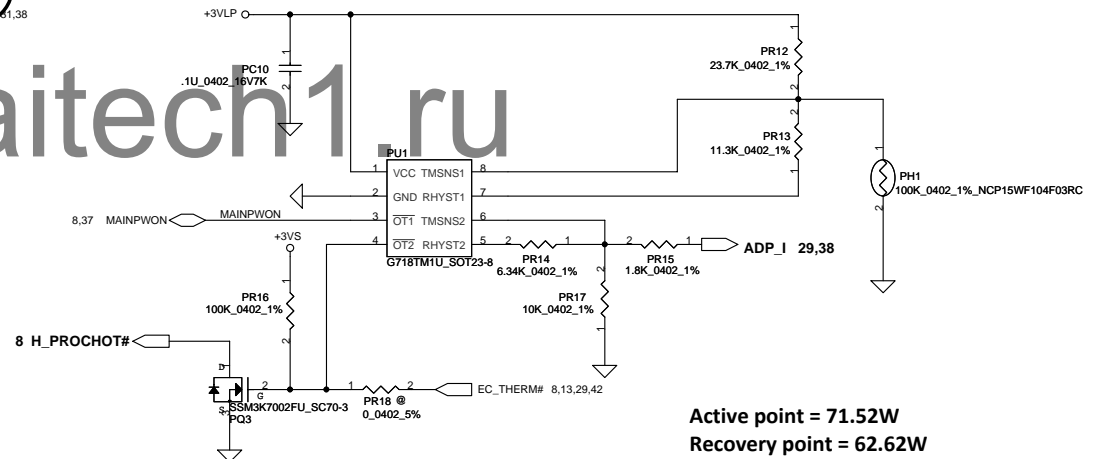


For KB930 --> Keep PU1 circuit  
(Vth = 0.825V)



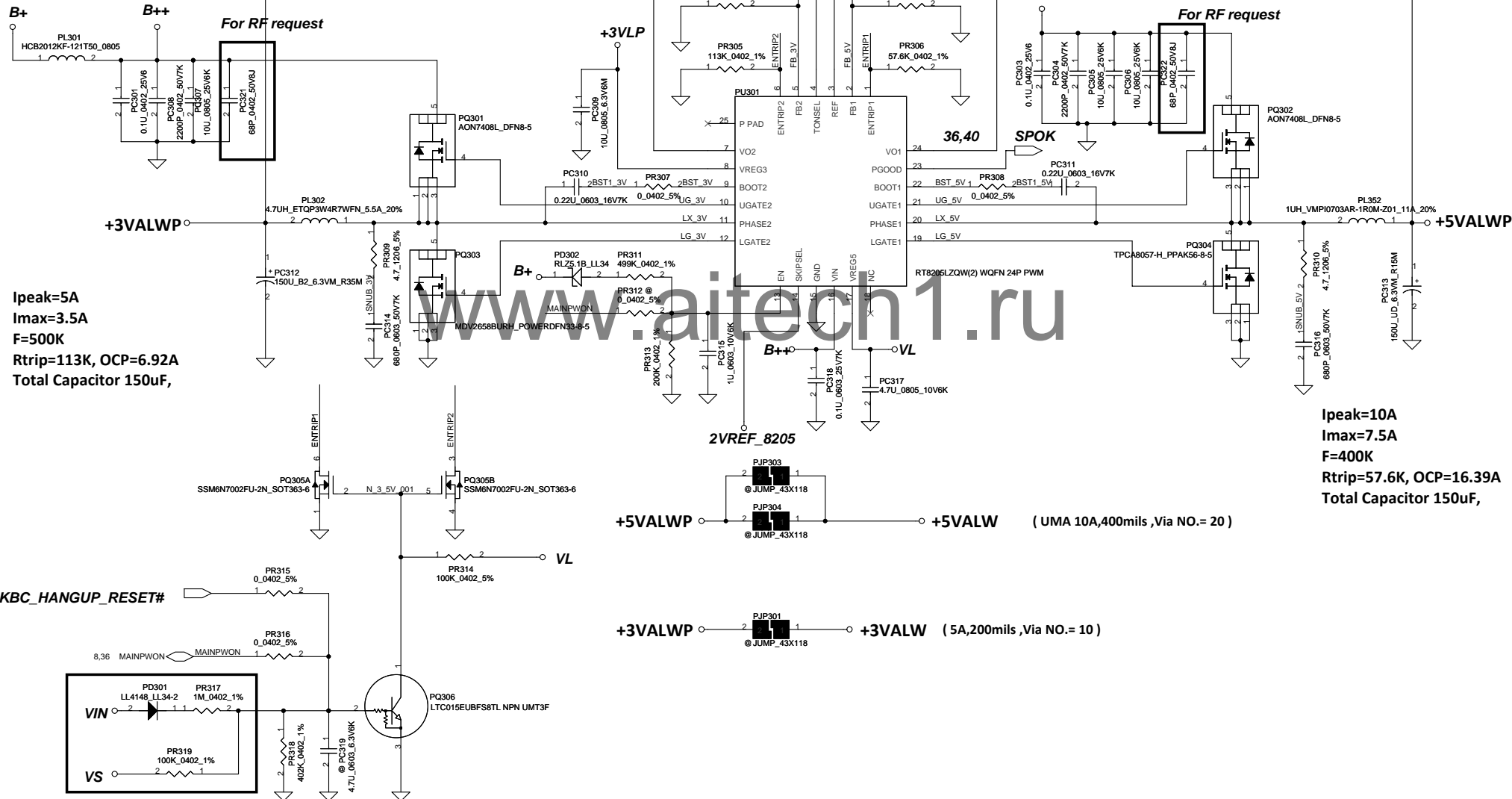
PH1 under CPU bottom side :  
CPU thermal protection at 90 +/-3 degree C  
Recovery at 56 +/-3 degree C

$$\begin{aligned} R_{set} &= 3 * R_{tmh} \\ R_{hyst} &= (R_{set} * R_{tml}) / (3 * R_{tml} - R_{set}) \\ R_{tmh} \text{ at } 90C &= 7.8K, R_{tml} \text{ at } 56C = 26.1K \\ R_{set} &= 3 * 7.8K = 23.4K \Rightarrow 23.7K \\ R_{hyst} &= (23.4K * 26.1K) / (3 * 26.1K - 23.4K) = 11.12K \Rightarrow 11.3K \end{aligned}$$



Active point = 71.52W  
Recovery point = 62.62W

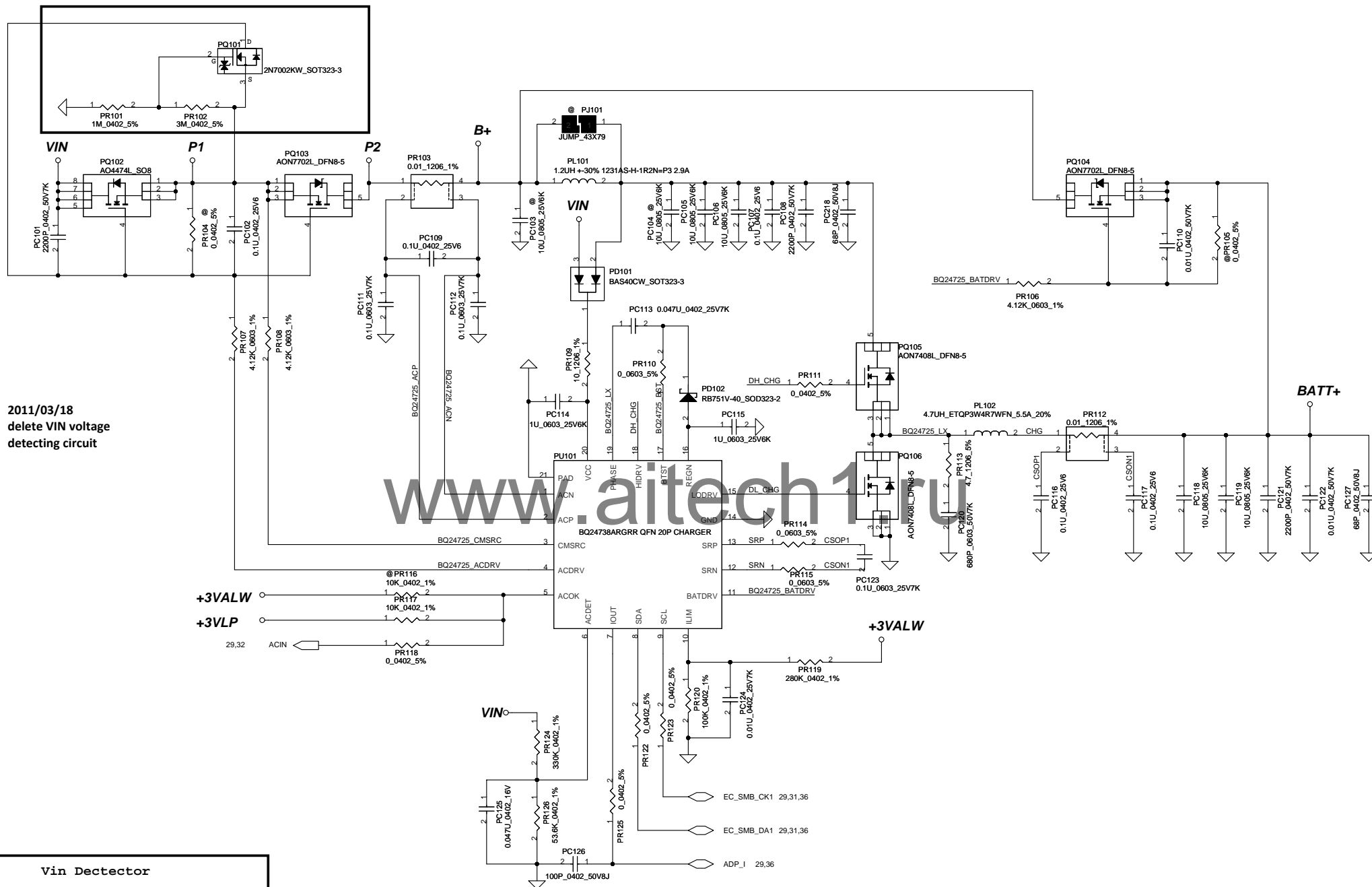
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|   |                    |                 |                          | Date: Tuesday, December 27, 2011 |
|   |                    |                 |                          | Sheet 36 of 46                   |



|   |                    |                 |            |                 |
|---|--------------------|-----------------|------------|-----------------|
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| Issued Date   | 2011/10/03         | Deciphered Date | 2014/12/31 | Document Number |
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| Date: Tuesday, December 27, 2011  |                    |                 |            | 0.1             |
| Sheet 37 of 46  |                    |                 |            |                 |

For KB930 --> Keep PD301, PR317, PR319

for reverse input protection



2011/03/18  
delete VIN voltage  
detecting circuit

#### Vin Detector

|       | Min. | Typ    | Max. |
|-------|------|--------|------|
| H-->L |      | 17.33V |      |
| L-->H |      | 16.98V |      |

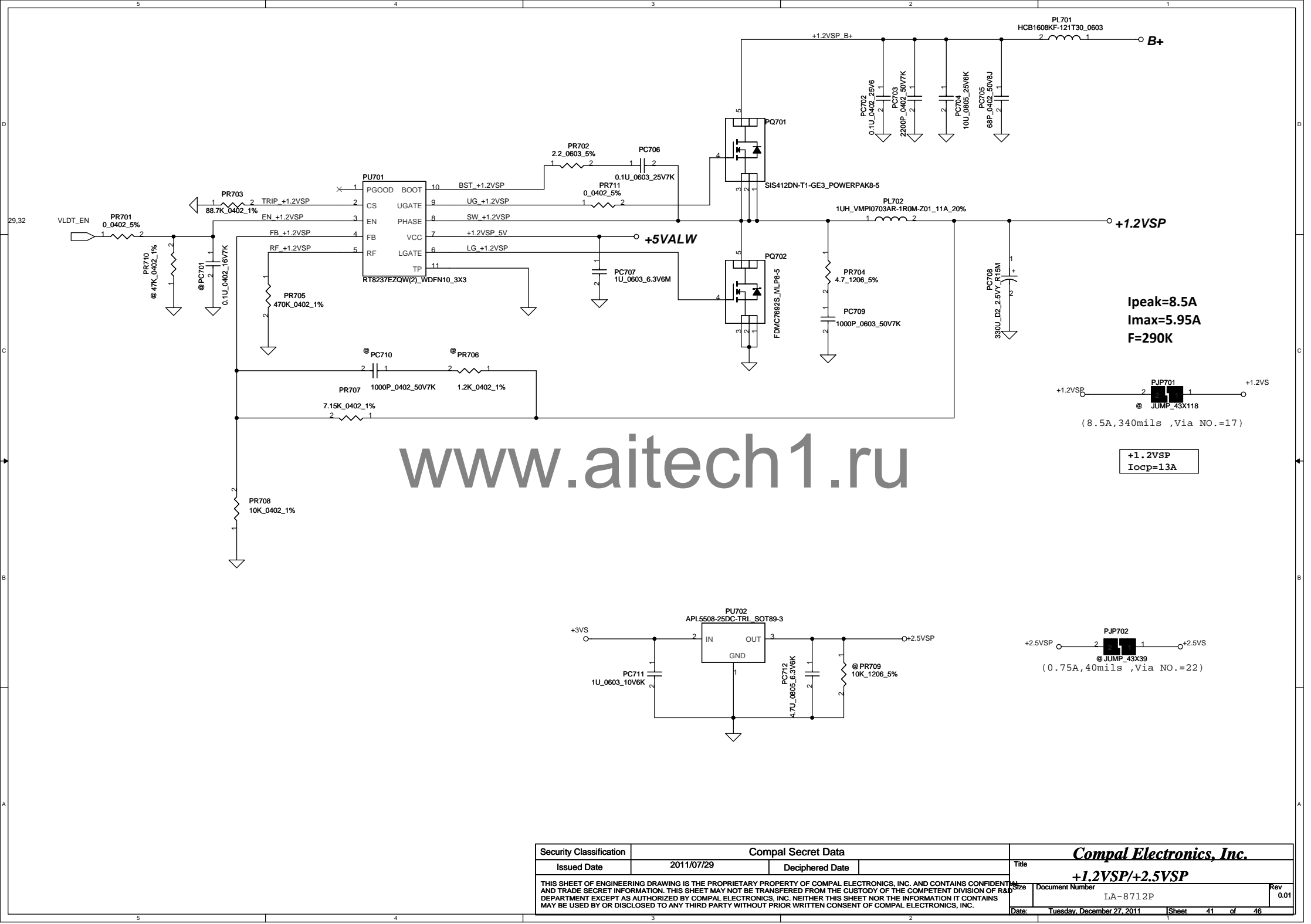
ILIM and external DPM  
4.36A

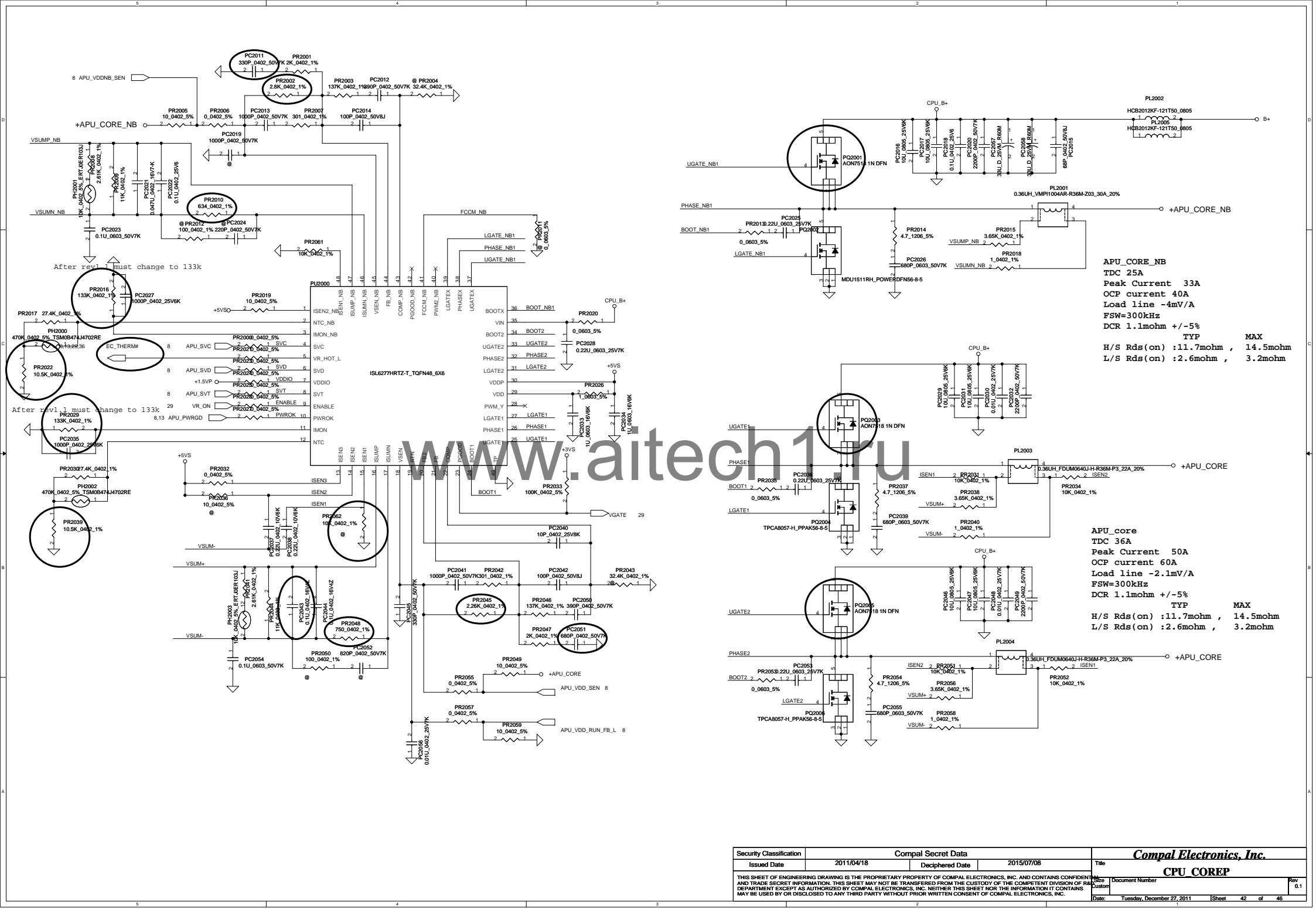
|   |            |                    |            |                          |                            |
|---|------------|--------------------|------------|--------------------------|----------------------------|
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|   |            |                    |            | Date:                    | Tuesday, December 27, 2011 |
|   |            |                    |            | Sheet                    | 38 of 46                   |
|   |            |                    |            | Rev                      | 0.1                        |











APU\_CORE\_NB  
TDC 25A  
Peak Current 33A  
OCF current 40A  
Load line -4mV/A  
FSW=300kHz  
DCR 1.1mohm +/-5%  
TYP  
H/S Rds(on) : 11.7mohm , 14.5mohm  
L/S Rds(on) : 2.6mohm , 3.2mohm

APU\_core  
TDC 36A  
Peak Current 50A  
OCF current 60A  
Load line -2.1mV/A  
FSW=300kHz  
DCR 1.1mohm +/-5%  
TYP  
H/S Rds(on) : 11.7mohm , 14.5mohm  
L/S Rds(on) : 2.6mohm , 3.2mohm

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